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Simulation Studies of Silica and High K Oxide Contained MOS Circuits (45nm, 32nm and 22nm) for Power Dissipation Reduction

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Abstract

Advances in semiconductor technology lead to the advancements in integrated circuits which have enhanced performance, reliability, cost effective, low power consumption, etc. To build a complex digital circuitry, millions of transistors are to be embedded onto a single chip to increase the performance and to improve the reliability of the electronic device. This paper aims at building of N-MOSFET, P-MOSFET, CMOS inverter and NAND gate using conventional SiO_2 oxide layer and high k oxide layer each of 45nm, 32nm and 22nm technologies respectively and to determine the percentage reduction in power dissipation using high k oxide layer in each device. The above mentioned devices are built using an online Predictive Technology Model tool and H-Spice simulation software and the simulated results are compared.

Index Terms: MOSFET, Inverter, NAND gate, Predictive Technology Model, H-Spice Tool, Power dissipation.

1. Introduction

A number of materials have been proposed to replace dielectric material in a MOSFET for future technology to reduce power dissipation in the device and hence in this work we develop a comparison of the percentage reduction in power loss using high K dielectric. The device model from Predictive Technology Models (PTM) of CMOS transistors' high K metal oxides in 45nm, 32nm and 22nm technology nodes are extracted to build up the required CMOS circuit in H-Spice user interface. H-Spice is a circuit simulation program which is used to perform transient analysis of several CMOS circuits. H-Spice enables the users to define parameters/expressions, provides modules of sub-circuits to include in the researcher's design, enables to

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parameterize the values when the module initialization is needed, arithmetic operations can be performed on the parameters and even the circuit models can be altered in the complexity to describe the behaviour of single transistors and CMOS circuits. The circuits which are modelled are simulated with the H-Spice program and in general, the obtained results are analyzed in AvanWaves tool which enables to display, analyze and print the simulations of H-Spice. Eventually scaling below 130nm, power dissipation becomes a primary issue while designing the CMOS circuits. In this paper, an attempt has been made to simulate and analyze power dissipation of N-MOS, P-MOS, CMOS inverter and NAND gate.

2. Modelling of the devices

N-MOSFET, P-MOSFET, CMOS inverter and NAND gate circuits of 45nm, 32nm and 22nm technology respectively using SiO_2 oxide layer and high K dielectric gate oxide are simulated in H-Spice simulator by extracting the model code from Predictive Technology Models (PTM) into the H-Spice library database in the corresponding file. The respective file is included in the H-Spice netlist for each device simulation. The model code for N-MOSFET containing SiO_2 oxide layer of 45nm, 32nm and 22nm are as given below,

```
.MODEL MODN NMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=3.9 EOT=1.1 W=500nm 45nm)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=3.9 EOT=1.1 W=500nm 32nm)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=3.9 EOT=1.1 W=500nm 22nm)
```

The model code for N-MOSFET containing high K oxide layer of 45nm, 32nm and 22nm are as given below,

```
.MODEL MODN NMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=27 EOT=1.1 W=500nm 45nm)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=27 EOT=1.1 W=500nm 32nm)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=27 EOT=1.1 W=500nm 22nm)
```

The model code for P-MOSFET containing SiO_2 layer of 45nm, 32nm and 22nm are as given below,

```
.MODEL MODN PMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=3.9 EOT=1.1 W=500nm 45nm)
.MODEL MODN PMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=3.9 EOT=1.1 W=500nm 32nm)
.MODEL MODN PMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=3.9 EOT=1.1 W=500nm 22nm)
```

The model code for P-MOSFET containing high K oxide layer of 45nm, 32nm and 22nm are as given below,

```
.MODEL MODN PMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=27 EOT=1.1 W=500nm 45nm)
.MODEL MODN PMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=27 EOT=1.1 W=500nm 32nm)
.MODEL MODN PMOS LEVEL=2 VTO=1.85 VS=0.09 KOX=27 EOT=1.1 W=500nm 22nm)
```

where VTO represents the threshold voltage, VS represents the static power input voltage, KOX represents the dielectric constant of oxide layer, EOT represents the equivalent oxide thickness in nm and W represents the device width. The '45nm.inc', '32nm.inc' and '22nm.inc' files are included in the netlists which are extracted from the PTM model where the by-default oxide thickness, t_{ox} as 1.1nm. Similarly, '45nmhighk.inc', '32nmhighk.inc' and '22nmhighk.inc' files are included in the respective H-Spice CMOS inverter netlists which are extracted from the PTM model where the by-default oxide thicknesses are $6.5x10^{-10}$m, $5x10^{-10}$m & $4x10^{-10}$m for 45nm, 32nm & 22nm technology respectively. Here, if we consider that the dielectric constant of the oxide layer as 27 (which is of Lanthana), the thickness of high K oxide layer (t_{HiK}) used in 45nm technology CMOS is obtained to be 4.5nm w.r.t SiO_2 contained 45nm technology CMOS. The thickness of high K oxide layer (t_{HiK}) used in 32nm technology CMOS is obtained to be 3.46nm w.r.t SiO_2 contained 32nm technology CMOS and the thickness of high K oxide layer (t_{HiK}) used in 22nm technology CMOS is obtained to be 2.76nm w.r.t SiO_2 contained 22nm technology CMOS. The thickness of high K oxide layer is calculated from the formula,

$$EOT = t_{ox} = \frac{3.9}{K\,(27)} * t_{HiK} \quad (1)$$

Thereafter, CMOS NAND gate circuits of 45nm, 32nm and 22nm technology containing SiO_2 and high K oxide layers are built in the H-Spice simulator using the NAND gate design code from PTM models. In the same way, '45nm.inc', '32nm.inc', '22nm.inc' files are included in the NAND gate H-Spice netlists which are extracted from the PTM model similar to the previously built CMOS inverter circuits.

3. Simulation Analyses

The task of modelling the MOSFETs and CMOS circuits is accomplished and the built circuits are simulated for the power dissipation analyses. In CMOS, the power dissipation mechanisms are divided into two types – dynamic and static power dissipation. Dynamic power dissipation occurs when the circuit is operational, i.e. when the circuit is performing some task on some data. Static power dissipation occurs when the circuit is inactive or in a power-down mode. Dynamic power dissipation can be further subdivided into three types - switched, short-circuit, and glitch power dissipation. All of these depend on the activity, timing, output capacitance, and supply voltage of the circuit. The repeated charging and discharging of the output capacitance is necessary to transmit information in CMOS circuits. The power consumption of a CMOS digital circuit can be represented as

$$P = fCV_{dd}^{2} + fI_{short}V_{dd} + I_{leak}V_{dd} \quad (2)$$

where f represents the clock frequency, C represents the average capacitance per clock cycle, V_{dd} represents the supply voltage, I_{short} is the short circuit current and I_{leak} represents the leakage current. The static power components are considered when there is no activity going on in the circuit and when they are biased to a particular state. The static power dissipation is due to the sub-threshold and reverse-biased leakage currents. Due to the down-scaling of threshold voltages, the sub-threshold leakage current is increasing and the sub-threshold current has a dependence on the threshold voltage.

Table 1. Table showing the %reduction in power loss in N-MOSFET

	NMOS					
	Dynamic Power Dissipation (W)			**Static Power Dissipation (W)**		
	MOS	**High K**	**%Reduction in power loss**	**MOS**	**High K**	**%Reduction in power loss**
45nm	219.93n	6.424n	97.07	36.44p	95.73f	99.73
32nm	365.12n	9.88n	97.29	83.30p	187.19f	99.77
22nm	616.59n	248.43n	59.70	169.11p	321.48f	99.80

The above table 1 shows the dynamic and static power dissipation of N-MOSFET using SiO_2 and high K oxide layers at 45nm, 32nm and 22nm technologies and their respective % reduction in power loss are calculated w.r.t. the power dissipation in SiO_2 oxide layer contained N-MOSFET.

Table 2. Table showing the %reduction in power loss in P-MOSFET

	PMOS					
	Dynamic Power Dissipation (W)			**Static Power Dissipation (W)**		
	MOS	**High K**	**%Reduction in power**	**MOS**	**High K**	**%Reduction in power**
45nm	374.38n	68.51p	99.98	77.01p	4.795f	99.99
32nm	633.99n	132.28p	99.97	259.96p	58.61f	99.97
22nm	894.22n	325.80p	99.96	487.84p	147.20f	99.96

The above table 2 shows the dynamic and static power dissipation of P-MOSFET using SiO_2 and high K oxide layers at 45nm, 32nm and 22nm technologies and their respective % reduction in power loss are calculated w.r.t. the power dissipation in SiO_2 oxide layer contained P-MOSFET. The dynamic power dissipation in the MOS containing high K oxide layer is low as observed in the above tables due to the electric field shielding capacity of the dielectric material in the MOSFET. The static power dissipation of high K contained P-MOSFET is lower than the SiO2 contained P-MOSFET but in the N-MOSFET we observe a rise in static power dissipation in the high K contained N-MOSFET. This increase is due to the reason that the electrons which are screened in the dielectric oxide layer start tunnelling towards the gate or source due to the applied gate voltage and this result in a slight increase in the power dissipation in N-MOSFET as the electrons are the majority charge carriers. From the tables 1 & 2 it can be observed that the maximum reduction in power dissipation occurs in 45nm technology P-MOSFET.

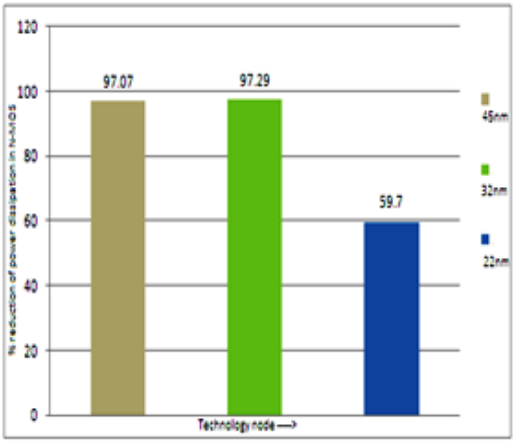

Fig. 1. % reduction of dynamic power dissipation in N-MOSFET

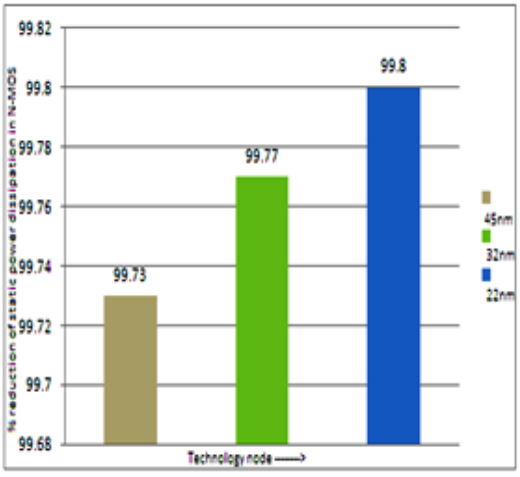

Fig. 2. % reduction of static power dissipation in N-MOSFET

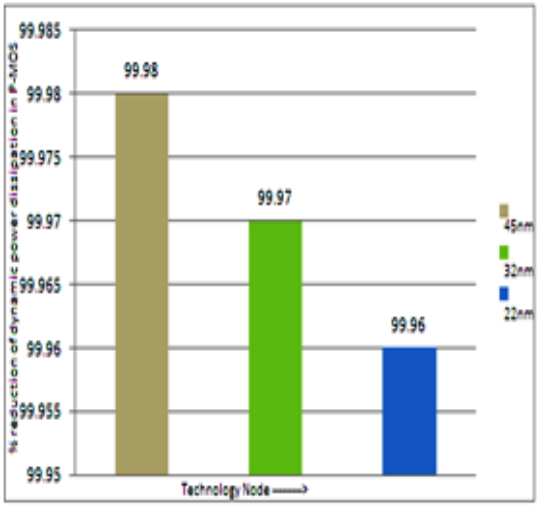

Fig. 3. % reduction of dynamic power dissipation in P-MOSFET

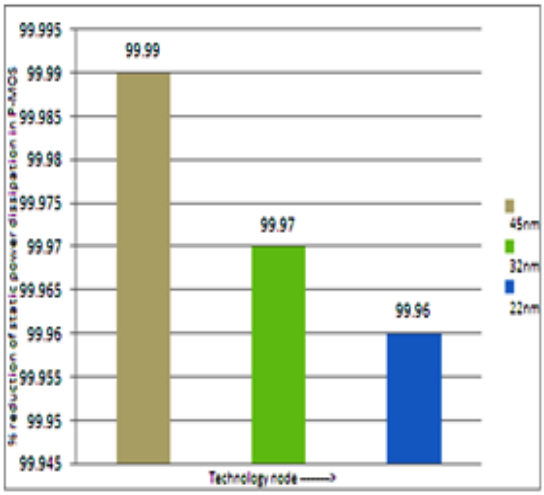

Fig. 4. % reduction of static power dissipation in P-MOSFET

Table 3. Table showing the %reduction of dynamic and static power loss in CMOS inverter

	Dynamic Power Dissipation (W)		**%Reduction in power**	**Static Power Dissipation (W)**		**%Reduction in power**
	CMOS	**High K**		**CMOS**	**High K**	
45nm	220.36n	6.412n	97.09	36.30p	96.09f	99.73
32nm	365.12n	9.48n	97.40	83.30p	186.48f	99.77
22nm	618.90n	247.5n	60.00	169.11p	213.4f	99.87

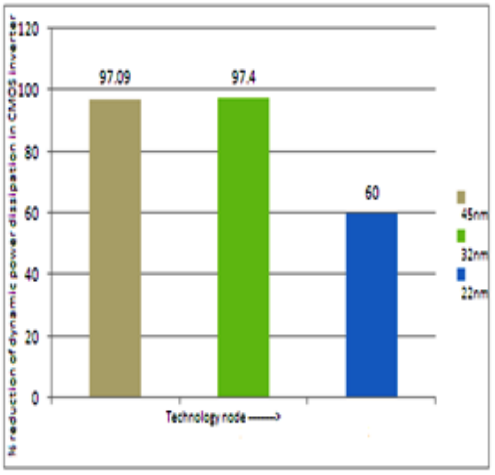

Fig. 5. % reduction of dynamic power dissipation in CMOS inverter

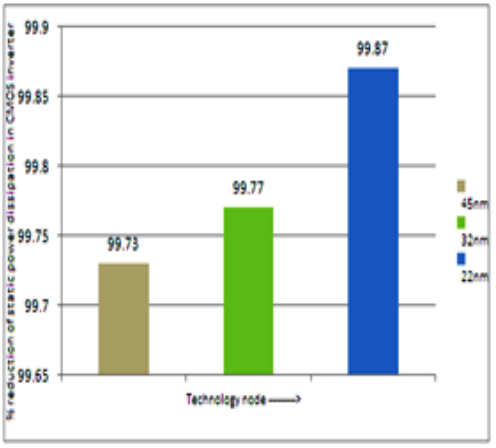

Fig. 6. % reduction of static power dissipation in CMOS inverter

Table 3 shows the % reduction of static and dynamic power dissipation in CMOS inverter circuit from which it can be observed that the maximum % reduction in power loss occurs in 32nm technology node.

Table 4. Table showing the % reduction of dynamic and static power loss in 2 input CMOS NAND gate circuit

	Dynamic Power Dissipation (W)		**%Reduction in power**	**Static Power Dissipation (W)**		**%Reduction in power**
	CMOS	**High K**		**CMOS**	**High K**	
45nm	409.88 µ	57.65n	99.98	537.09n	325.168p	99.93
32nm	690.93 µ	271.816n	99.96	631.169n	414.289p	99.93
22nm	821.40 µ	351.27n	99.95	720.996n	608.768p	99.91

Table 4 shows the % reduction of static and dynamic power dissipation in CMOS NAND gate circuit from which it can be observed that the reduction of power loss occurs in the circuit in which high K insulator layer is contained and the maximum % reduction in power loss occurs in 45nm technology node.

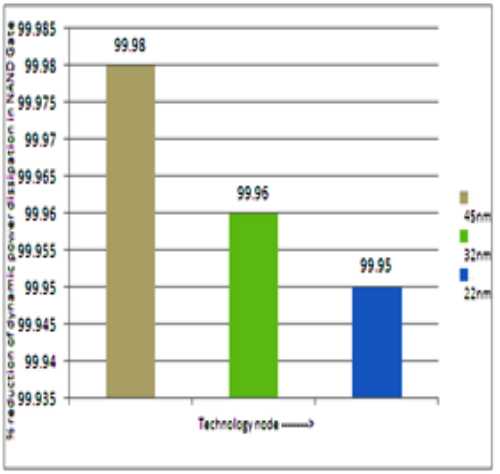

Fig. 7. % reduction of dynamic power dissipation in CMOS NAND gate circuit

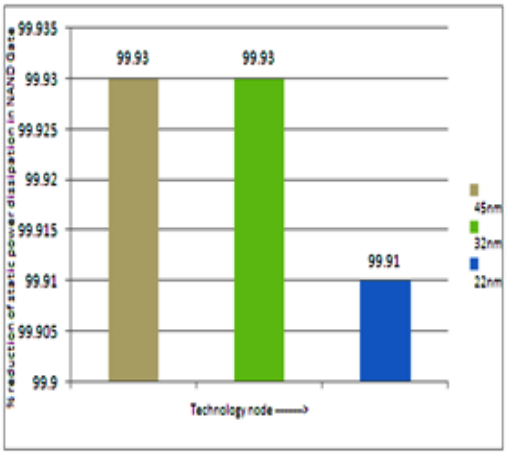

Fig. 8. % reduction of static power dissipation in CMOS NAND gate circuit

4. Conclusion

Introducing high K material in the MOS technology is a way to reduce the power dissipation of the circuit in 45nm, 32nm and 22nm technology nodes. This is very efficient technique as the above simulated MOSFETs and CMOS circuits are to be embedded into a chip through which the overall power dissipation would drastically decrease leading to a lower heating of the electronic device. The high K contained MOS circuits also reduces the leakage current which ultimately increases the device performance and power back-ups. Hence high K power gating is the most feasible solution to reduce the power dissipation effects.

References

[1] Frank Anthony Hurtado and Eugene John, "A Comparative Analysis Of Leakage Reduction Techniques In Nanoscale CMOS Arithmetic Circuits", Proceedings of the 2014 ASEE Gulf-Southwest Conference Organized by Tulane University, New Orleans, Louisiana.

[2] P. Kapur, R. S. Shenoy, A.K. Chao, Y. Nishi and K. C. Saraswat, "Power Optimization of Future Transistors and a Resulting Global Comparison Standard", 2004, 0-7803-8684-1, IEEE.

[3] Ebrahim Nadimi, Philipp Plänitz, Rolf Öttking, Karsten Wieczorek, and Christian Radehaus, "First Principle Calculation of the Leakage Current Through SiO_2 and SiO_xN Gate Dielectrics in MOSFETs", 2010, 57, 3, IEEE Transactions On Electron Devices.

[4] W. Tsai, N. Goel, S. Koveshnikov, P. Majhi, W. Wang, "Challenges of integration of high-j dielectric with III–V materials", 2009, 86, 1540–1543, Microelectronic Engineering, Science Direct.

[5] Yudong Kim, Gabriel Gebara, Michael Freiler, Joel Barnett, Deborah Riley, Jerry Chen, Kenneth Torres, JaeEun Lim, Brendan Foran, Fred Shaapur, Avinash Agarwal, Patrick Lysaght, George A. Brown, Chadwin Young, Swarnal Borthakur, Hong-Jyh Li, Billy Nguyen, Peter Zeitzoff, Gennadi Bersuker, David Derro, Renate Bergmann, Robert W. Murto, Alex Hou, Howard R. Huff, 'Eric Shero, 'Christophe Pomarede, 'Michael Givens, 'Mike Mazanec, and 'Chris Werkhoven, "Conventional n-channel MOSFET devices using single layer HfO2 and ZrO_2 as high-k gate dielectrics with polysilicon gate electrode", 2001, 01, 0-7803-7050-3, IEEE.

[6] Marlia Morsin, Mohd Khairul Amriey, Abdul Majeed Zulkipli and Rahmat Sanudin, "Design, Simulation and Characterization of 50nm p-well MOSFET Using Sentaurus TCAD Software", Proceedings of MUCEET, 2009.

[7] Marlia binti Morsin, Mohd Khairul Amriey, "Designing and Characterization of 60nm p-well MOSFET Using Sentaurus TCAD Software", 2010, 10, 978-1-4244-7406-6, IEEE.

[8] Xinlin Wang, *Ghavam Shahidi, Phil Oldiges and Mukesh Khare, "Device Scaling ofHigh Performance MOSFET with Metal Gate High-K at 32nm Technology Node and Beyond", 2008, 08, 978-1-4244-1753-7, IEEE.

[9] Chris A. Mack, "Fifty Years of Moore's Law", 24, 2, IEEE Transactions On Semiconductor Manufacturing, 2011.

[10] Jack C. Lee, H. J. Cho, C. S. Kang, S. Rhee, *Y.* H. Kim, R. Choi, C. *Y.* Kang, C. Choi, M. Abkar, "High-K Dielectrics and MOSFET Characteristics", 2003, 03, 0-7803-7872-5, IEEE.

[11] Gang He, Liqiang Zhu, Zhaoqi Sun, Qing Wan, Lide Zhang, "Integrations and challenges of novel high-k gate stacks in advanced CMOS technology", Progress in Materials Science, 2011, 56, 475-572, Science Direct.

Authors Profiles

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V. S. K. Reddy – Dr. V.S.K. Reddy, Principal, Malla Reddy College of Engineering & Technology was graduated with B.Tech. in Electronics and Communication Engineering (ECE), S.V. University and M.Tech in ECE, JNT University, Hyderabad. He is highly versatile with multidisciplinary specializations in Electronics & Communications and Computers Science & Engineering. He has outstanding contribution with more than 35 Publications in the National and International reputed Conferences and Journals. He is a fellow of IETE, Member of ISTE & Member of IEEE. He was awarded as "Best Teacher" in three consecutive Academic years with citation and cash award. He is the recipient of "India Jewel Award" for outstanding contribution to the research in the field of Engineering and Technology. He is a Member of Board of Studies for M.Tech program at Sreenidhi Institute of Science & Technology, Hyderabad which is in collaboration with M/s. Synopsis-SEER Academy, USA. He is also a member of Board of Studies, ECE & ETM, JNT University, Hyderabad. He is Proactive member in Governing Boards of several engineering colleges.

M.V. Manasa – M.V. Manasa completed her B.Tech in Electronics and Communication Engineering and M.Tech in Nano Technology from Jawaharlal Nehru Technological University Hyderabad. She worked on synthesis and simulation of high K dielectric materials and has publications in many peer reviewed national and international journals. She is recently awarded by DST-INSPIRE Fellowship and her present research is oriented towards synthesis, characterization of nano lanthanides, MOSFET and nano electronic devices simulation studies.

K. Venkateswara Rao – Dr. K. Venkateswara Rao completed his M.Sc. (Physics) from Central University of Hyderabad in the year 1997 and is a gold medallist. He was UGC-CSIR (NET) qualified in the year 2001 and was awarded his Ph.D. from Central University of Hyderabad in the year 2008. He completed his M.Tech. in Computer Science Engineering from Jawaharlal Nehru Technological University Hyderabad and is presently working as Associate Professor in Nano Technology at CNST, JNT University Hyderabad. He has several research publications in international & national journals, national & international conferences and also conducted many workshops. He is recognized as DST committee member, BOS chairman for B.Tech – Mechanical Engineering (Nano Technology), Red Cross Life member, BOS member at JNTUH (physics), JNTUK (physics), JNTUA (physics), KL University (NanoTechnology). Dr. K. Venkateswara Rao is also member of Nano Technology subcommittee, Andhra Pradesh Chambers of Commerce and Industry (FAPCCI), regular writer for first year B.Tech Engineering physics material for sakshi, bavitha website and guest faculty of National institute of fashion technology. He has guided more than 60 PG projects, supervising 8 Ph.D. students and is also working on the projects which are funded by UGC and DST-SERB. His current areas of research specialization include Synthesis of and characterization of nano materials, fabrication of thin films and characterization, bio-Medical application of nano materials, DMS nano materials, Pulsed electro fabrication on silicon substrate nano lanthana and characterization for future CMOS technology and Seed germination using nano materials.

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