Design of Low Voltage and High-Speed BiCMOS Buffer for Driving Large Load Capacitor

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Abstract

BICMOS circuits are interesting for designers when a high speed output driver is required especially in I/O circuits. Buffer is an important block in high speed circuits, so designing a buffer with high drive capability has a great effect on circuits with large load capacitor. This paper presents a new BiCMOS buffer which uses 32nm technology node for CMOS transistors and 0.18um technology node for BJT transistors. The proposed buffer operates properly in voltage ranges from 0.8v to 1.5v. The capacitor range is from 0.5pf to 200pf; the overshoot of the output in this capacitor range is less than 10% of the supply voltage that is negligible. The proposed design has improvements in delay for about %88 respectively compared to similar CMOS buffers with high capacitor values.

Index Terms: Buffer, BiCMOS, High load, Capacitor, Low power, Inverter.

1. Introduction

In recent years, the advantages of CMOS over BiCMOS technology such as speed, power, and cost have been proven. Hence, many researches focus on investigating the aspects of low voltage, low power, and high speed for this dominant semiconductor technology. Using lower power supply voltage is one of the major solutions for decreasing device power consumption. Nowadays, circuits are designed to operate within the domains near the threshold-voltage as a result of these efforts to reduce supply voltage (V_{th}) [1] [2].

Circuits with high current capability which use Bipolar and CMOS technologies combination, named BiCMOS. BiCMOS technology is beneficial especially when a high speed output driver is required. The circuit

designers' ultimate goals are to scale down supply voltage, and decrease the propagation delay along with power consumption concurrently. Since these parameters are not achievable at the same time, so making a tradeoff among them should be considered [3] [4]. It is worth noting that high capacitive loads are often appeared in I/O circuits [10][11]. Buffers are crucial blocks in high speed circuits; therefore, a buffer with high drive capability would be significantly effective for circuits with large load capacitor [2] [5] [7] [8]. In this paper a BiCMOS buffer is proposed with a supply voltage of 0.8v~1.5v.

Due to the fact that the recently suggested designs for CML buffers in enjoy a great deal of advantages, since these buffers have high static power consumption, suggesting a circuit with a low rate of static power consumption can be of great interest. To improve the proposed design it can be also changed into tapered buffer in order to not only reduce the power consumption, but also decrease the delay of the circuit. The proposed scheme in this paper, can be used to design the current mode BiCMOS circuit which can be applied in ripple adder circuits. [5] [8]

The rest of the paper is organized as follows: the former investigations about BiCMOS inverter gate designs are demonstrated in Section 2. Section 3 proposes a new BiCMOS design which will be optimized. The simulation results and comparisons are presented in section 4. Finally, Section 5 comes with the conclusion.

2. Related Work

Over the past decades, different BiCMOS circuits were presented. Power, delay, power delay product (PDP), high swing capability and overshoot are among major parameters for evaluating BiCMOS circuits. Researches on designing of BiCMOS circuits mainly focus on high swing designs besides low power circuits. For instance, high swing circuits using resistance elements are not desirable due to their high power consumption. In BiCMOS circuits, overshoot values under 10% of supply voltage are negligible.

Some BiCMOS inverters have been studied in [4], [6], [8] and [9]. In this paper two example of BiCMOS inverter circuits are discussed and compared to each other as conventional designs which are shown in Fig. 1 (a) and (b). The circuit operation of Fig. 1 (a) is described as following. If the input voltage is '0', the transistor P1 is ON, where N1 and N2 are OFF. Therefore V_{DD} is transferred to B1 node through P1. Logic '1' on B1 turns the Q1 ON and causes V_{out} to be '1'. High voltage on B1 node turns the N3 transistor ON, then Q2 is being OFF. When the input voltage equals to 'V_{DD}', P1 is OFF and N1 and N2 are ON. Consequently V_{GND} is passed on B1 node through N1 transistor. As V_{B1} = '0', so Q1 and N3 are turned OFF. Consequently transistor Q2 is ON, C1 Capacitance is discharged and causes V_{out} to be logic '1' [4] [6] [8].

Fig.1 (b) shows another BiCMOS inverter design. The circuit works as below. When input voltage equals to '0', transistor P1 is ON and transistor N1 is OFF. So transistors Q_1 and N2 are ON and output voltage will be logic '1'. When input voltage is equal to '1', N1 is ON. So Q_1 is being OFF and P2 and Q2 are ON. Hence, C1 capacitance is discharged and consequently output voltage is equal to '0' [9].

The functionality of these circuits requires that one of the BJTs to be OFF to avoid an unknown output caused by competing two BJTs to concurrently pull down and up the output. These circuits which have been used as inverter gates have the following specifications: the minimum supply voltage is 3.3v. In addition when the output logic is '1' the output voltage will be decreased by the amount of BJT threshold voltage.

Other proposed designs in recent years, which is mentioned in the introduction, is CML buffers. Although they have acceptable capabilities, but according to static power consumption, they are not in desirable condition. Therefore, there are many efforts have been made to reduce the static power by designing the improved schemes. Generally, in order to increasing the speed of buffers, the sequence buffers are used, which are called tapered buffers, and they are in the cascaded buffers category. This method is exploited for CML buffers and conventional CMOS buffers. [5] [10] [12].
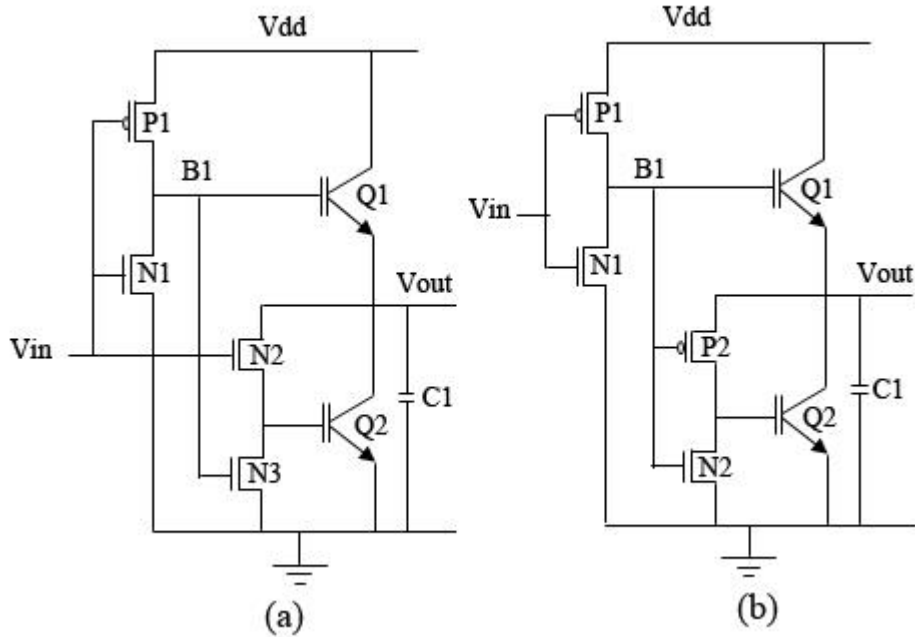
Fig.1. (a) A Conventional inverter Circuit. (b) An inverter which Uses PMOS Transistor.

3. HDBiCMOS (High Drive BiCMOS) buffer

The HDBiCMOS circuit, as a kind of BiCMOS buffer, uses cascaded CMOS and bipolar inverters. Fig. 2 illustrates the proposed BiCMOS buffer that its operation is described as follows: if $V_{IN}=0$, P1 and Q2 transistors will be ON, so capacitor C1 will be charged, and capacitor C2 will be discharged and voltage output would be equal to '0'. When the input voltage is V_{DD}, N1 is ON and C1 will be discharged. So Q1 is ON and the output logic will be '1'.

The problem of such a design is the voltage level variation of node C. when C is in high voltage level, so Q2 is ON and the voltage level of C has been decreased gradually and this causes that Q1 will be turning ON. Consequently this problem make the output voltage will be unknown. This problem also happened similarly when the voltage level of C is low.

The only solution for this problem is to prevent Q1 and Q2 to be simultaneously in active region. To do so, we suggest reducing the supply voltage. By applying lower supply voltages, when the voltage level of C is high, Q2 is ON and by decreasing the voltage level of C, Q1 is still OFF since $V_{EB}(Q1) < V_{th}(Q1)$. When the voltage level of C is low, Q1 is ON and Q2 is OFF and will be remained OFF since $V_{BE}(Q2) < V_{th}(Q2)$.

Cascading two CMOS inverters results in a CMOS buffer (Fig. 3). These circuits are compared according to previously mentioned parameters. Compared features include: power, propagation delay, power delay product (PDP) and the correctness of circuit functionality. As long as load capacitor value is small, both the BiCMOS and CMOS buffers have similar performances. By raising the lead capacitor values the output delay will be increased. Where, the CMOS buffer cannot work properly, the BiCMOS buffer have a perfect functionality.
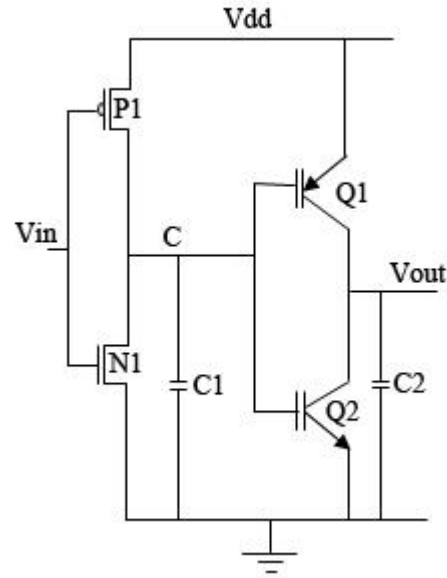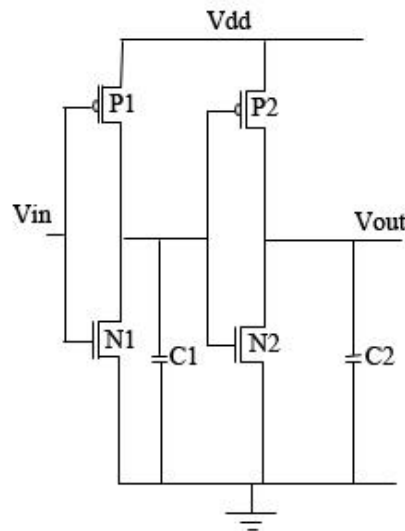
Fig.2. The Proposed Bicmos Buffer (HDBiCMOS)

Fig.3. CMOS Buffer Circuit

As explained above, the circuits in Fig. 1 (a) and (b) operate with at least 3.3v supply voltages. In the proposed buffer reducing the voltage would solve the problem at C node; so the output of circuit would be acceptable. Regarding the supply voltage of modern circuits, against classic BiCMOS circuits, the proposed buffer operates perfectly in modern ICs. In order to reduce the buffer delay in large load capacitor, the proposed buffer was modified. In the modified buffer by adding an inverter we can charge and discharge the capacitor C1 faster. So we can achieve less delay.
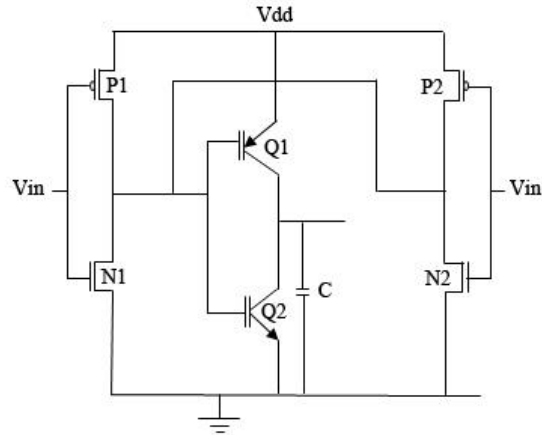
Fig.4. Proposed Modified HDBiCMOS Buffer

4. Simulation Result

The proposed HDBiCMOS circuit and the other previous circuits are simulated and compared. It is worth mentioning that TSMC 0.18um technology for BJT transistors and 32nm technology for CMOS transistors are employed. Fig. 5 illustrates the transient respond of CMOS versus HDBiCMOS buffer outputs. The simulations are performed in the 1V supply voltage and different load capacitors. HDBiCMOS circuits have significantly better functionality and less delay than CMOS circuits. HDBiCMOS circuit has bipolar transistors that provide bigger current that increase driving capability and faster charging and discharging for capacitors. According to the simulation results, by increasing the capacitor value more than 60pf, the CMOS buffer delay will be raised. Moreover, for large load capacitors, the CMOS buffer could not fully charges the capacitor, consequently resulting in output failure. A comparison of power, delay, and PDP values between HDBiCMOS and CMOS buffers is demonstrated in table 1. The capacitor values are 30pf, 60pf, 65pf, and 100pf. The output of CMOS buffer circuit using 1V supply voltage with capacitor values more than 60pf will be failed.

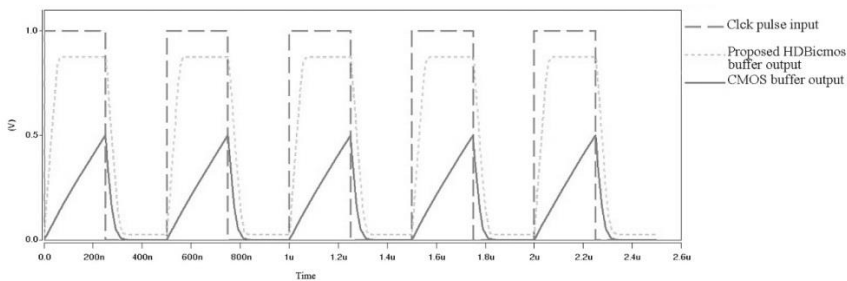Fig.5. Output Comparison between HDBiCMOS Proposed Buffer and CMOS Buffer.

The comparison of delay and PDP values of both CMOS and proposed BiCMOS buffers in different supply voltages are shown in Fig. 6. As it is illustrated in the Fig. 6 by decreasing the supply voltage, PDP of the proposed buffer circuit is better than CMOS buffer, but delay of proposed buffer is entirely better than CMOS buffer.

Delay, power consumption and PDP of the proposed HDBiCMOS buffer are compared to the modified proposed HDBiCMOS buffer. Based on the simulation results, delay at capacitor values of 10pf to 200pf are evaluated, which shows 38% improvement at least compared to the proposed HDBiCMOS buffer circuit (Table 2). To improve proposed circuit instead of using transistors with W/L ratio size on the first stage of the circuit, we can use transistors with W/2L ratio size on two stages as it is illustrated in Fig. 4. The main reason for this improvement is prevents the formation of large gate capacitor.

Table 1. Comparison of BiCMOS and CMOS in terms of Power, Delay, and PDP

Capacitor Value	Circuit	Delay(*e-8)	PDP(*e-11)	Power(*e-4)
100pf Load Capacitor Value	proposed HDBiCMOS buffer	8.11	2.11	2.60
	CMOS buffer	Failure		
65pf Load Capacitor Value	proposed HDBiCMOS buffer	3.32	1.48	4.47
	CMOS buffer	Failure		
60pf Load Capacitor Value	proposed HDBiCMOS buffer	4.90	1.14	2.33
	CMOS buffer	25.2	1.21	0.476
30pf Load Capacitor Value	proposed HDBiCMOS buffer	1.56	0.614	3.92
	CMOS buffer	12.6	0.650	0.517

	1.5v	1.2v	1v
■ Delay CMOS	1.38E-07	1.82E-07	2.49E-07
▨ Delay HDBiCMOS	1.70E-08	2.07E-08	3.07E-08

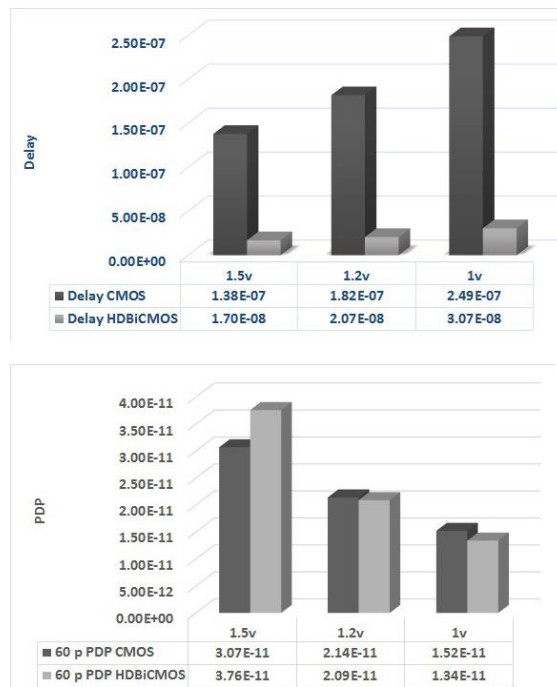|	1.5v	1.2v	1v
■ 60 p PDP CMOS	3.07E-11	2.14E-11	1.52E-11
▨ 60 p PDP HDBiCMOS	3.76E-11	2.09E-11	1.34E-11

Fig.6. The Delay and PDP Comparison between HDBiCMOS and CMOS Buffers.

Table 2. Consumption of CMOS Buffer and Proposed HDBiCMOS in terms of Propagation Delay, Power Consumption and PDP.

CL(pf)	Proposed HDBiCMOS Buffer			modified Proposed HDBiCMOS Buffer		
	Propagation Delay(S)	Power Dissipation (W)	PDP (WS)	Propagation Delay(S)	Power Dissipation (W)	PDP (WS)
20	1.91×10^{-8}	2.06×10^{-4}	3.95×10^{-12}	1.10×10^{-8}	3.68×10^{-4}	4.08×10^{-12}
40	3.30×10^{-8}	2.20×10^{-4}	7.27×10^{-12}	2.07×10^{-8}	3.82×10^{-4}	7.91×10^{-12}
60	4.90×10^{-8}	2.33×10^{-4}	1.14×10^{-11}	3.07×10^{-8}	3.95×10^{-4}	1.21×10^{-11}
80	6.51×10^{-8}	2.48×10^{-4}	1.61×10^{-11}	4.08×10^{-8}	4.08×10^{-4}	1.66×10^{-11}
100	8.11×10^{-8}	2.60×10^{-4}	2.11×10^{-11}	5.09×10^{-8}	4.22×10^{-4}	2.15×10^{-11}
120	9.71×10^{-8}	2.74×10^{-4}	2.66×10^{-11}	6.09×10^{-8}	4.34×10^{-4}	2.65×10^{-11}
140	1.13×10^{-7}	2.88×10^{-4}	3.26×10^{-11}	7.10×10^{-8}	4.48×10^{-4}	3.18×10^{-11}
160	1.29×10^{-7}	3.02×10^{-4}	3.90×10^{-11}	8.11×10^{-8}	4.62×10^{-4}	3.74×10^{-11}
180	1.45×10^{-7}	3.15×10^{-4}	4.58×10^{-11}	9.12×10^{-8}	4.74×10^{-4}	4.32×10^{-11}
200	1.61×10^{-7}	3.28×10^{-4}	5.30×10^{-11}	1.01×10^{-7}	4.87×10^{-4}	4.93×10^{-11}

5. Conclusion

Decreasing the delay value beside power consumption are among the main challenges in designing circuits. On the other hand, increasing the load capacitor value results in significant increase in delay and power consumption value. Therefore designing a buffer and placing it in circuit's output is of important factors since they are substantial in increasing the diving capability. The buffers presented in this paper are BiCMOS which operate properly in voltage range of 0.8v to 1.5v. Such buffer enables charging and discharging capacitors with a low delay value. According to the simulation results with HSPICE simulator, the proposed circuits respond better with capacitor range between 0.5pf to 200pf. Moreover, the delay value could also be decreased more by modified circuit.

The proposed circuit enjoys less delay value and better performance in comparison to the other similar circuits. It also improves the delay value about 88% compared to CMOS circuits for large capacitor value. However it is worth mentioning that, with increasing the capacitor value up to 200 pf and more, CMOS buffer circuits will have the lower frequency (about 25%) than BiCMOS. In other words BiCMOS circuits operating frequency range is higher than the CMOS circuits.

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