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Wide Tuning Range CMOS VCO

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Abstract

A communication system requires a highly stabilized frequency; LC and RC oscillator are two wide option for frequency generation. Performance of an LC oscillator suffers from leakage, area, noise etc compare RC oscillator. Voltage controlled oscillator (VCO) is preferred category if RC oscillator to generate high oscillator frequency. VCO contains odd number of delay stage cascaded together; output frequency strongly depends on switching threshold of individual stages. A 3 stage current starved VCO can generate upto 0.6 Ghz; this work is focused around body bias technique to increase frequency without increasing number of delay stage. Oscillation frequency has been controlled by bulk terminal of PMOS and NMOS individually and by means of adaptive body bias network. Cadence spectre based simulation result at CMOS 90nm shows that by reverse biasing of PMOS obtained frequency is 1.2GHz-10.01GHz with tuning range of 95% while biasing of NMOS generate frequency of 500MHz- 12.5GHz with tuning range capability of 96%. This design presents high frequency with wider tuning range and optimum reduced power by which this oscillator design can be used in different band of communication.

Index Terms: Ring oscillators, Voltage-controlled oscillators, Frequency, Phase noise, Tuning, Bandwidth.

1. Introduction

Voltage controlled oscillator is commonly investigated as it is a crucial circuit of phase locked loop (PLL), clock and data recovery circuits (CDR), Radio Frequency application**.** Ring oscillator is the primary component of VCO; a cascade combination of delay stages connected as closed loop. In satellite / microwave communication clock data recovery unit at receiver restore the clock from received data with the help of PLL [1, 2]. Ring oscillator is the heart of VCO it generates oscillating frequency in specific band (up to 30 GHz). In

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this work current starved topology has been consider as basic element for delay calculation [14]; it limits the current to the inverter for charging and discharging of load there by controlling the stage delay and oscillation frequency. Current starved ring oscillator can generate frequency 4 GHz applicable for L, S and C-band. In this work frequency range tried improve up to 12.5 GHz for K-band application using body biasing technique. Body biasing of MOS effectively alter the threshold voltage it significantly improves the delay stage result in high frequency.

A current starved topology shown in Fig1, it is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The main control on the inverter chain is of V_{inVCO} to modify the current that flow from the N1 and P1. The current from these transistors due to direct connection of M5 with M1 along with following transistor and M6 with M4 followed by transistor in series mirror the current in each. Change in the control voltage induces by change in inverter current. V_{inVCO} modulates the turn on resistance of pull down transistor M1 and through the current mirror, the pull-up transistor M6 [3-7]. Large value of V_{inVCO} allows a large current to flow, producing a small resistance and a small delay. Cadence Spetre based simulation justify that a current starved ring oscillator can produce frequency 626 MHz at Vdd 1V.

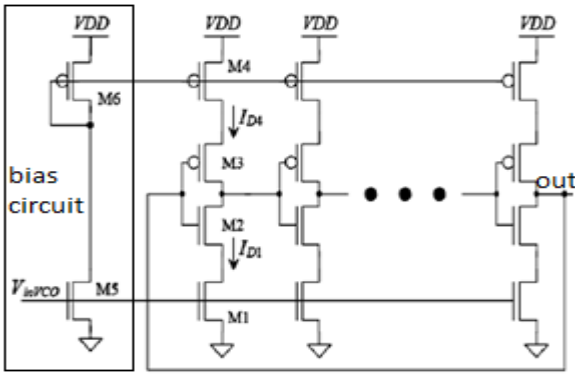

Fig.1. Current Starved Ring Oscillator [8, 9]

Oscillator's frequency primarily depends in threshold voltage of MOS; body biasing is one of technique through which threshold voltage of particular MOS can be varied; usually PMOS body terminal should connect to maximum supply and NMOS body to minimum ground; but additional voltage at body terminal vary the threshold voltage by eqn (1). Threshold voltage of MOS increases by reverse biasing and decrease with forward biasing [1, 2, 11]. Effect of body voltage over represented by, γ is body bias factor, Vth decrease for higher V_{SB} and decreases for lower V_{SB}.

$$V_{Th} = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \quad (1)$$

1.1. Organization of paper

The second section of the paper elaborate current starve ring oscillator with PMOS and NMOS body bias individually and their effect over frequency and other parameter explored. Section-3 of the paper incorporates conclusion and possible future work.

2. Current Starve VCO with Body Bias

A ring oscillator frequency can enhance by an additional supply at body terminal, reverse biasing body

reduces Vth in case of PMOS and increase in case of Vth. Variation in Vth configure delay of MOS, in this section effect of reverse bias over frequency has been explored.

2.1. Current Starve Ring Oscillator with PMOS Body Biasing

Fig2 shows a 3 Stage current starved topology of ring oscillator. In the presented VCO, substrates of PMOS have been connected to dc supply which is kept at optimum value 0.5V, Vctrl is varied in the range of 0 to1V, and Simulations have been carried out using cadence spectre based on CMOS 90nm technology at supply 1V. PMOS reverse body bias increase threshold voltage and leads to high oscillation frequency. Positive bulk terminal input reduced sub threshold leakage current and minimizes the power dissipation [8, 9, 10].

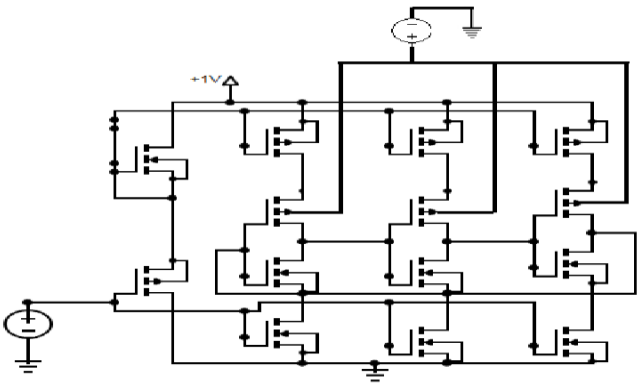

Fig.2. Current Starved Ring Oscillator with PMOS Body Biasing

On current increases with increasing body voltage increases upto V_{SB}=0.5 V. Further increase in the body voltage decrease the value of drain current (I_{DS}). Fig3 shows variation of frequency w.r.t Vctrl keeping body voltage at optimum value 0.5V. Current starve VCO with PMOS Body Biasing voltage can achieve maximum frequency oscillation frequency 1.2 to 11GHz while Vctrl ranges from 0-1V at body voltage V_{SB} 0.5V. Power consumption of the above circuit is 30uw.

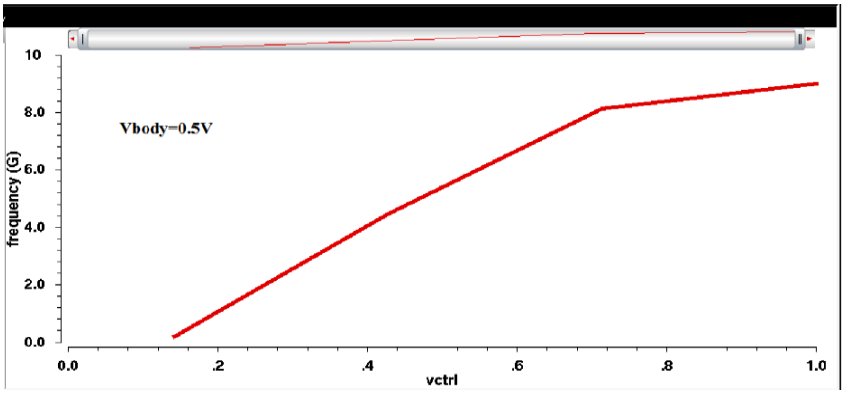

Fig.3. Frequency Variation with Vctrl at Body Voltage 0.5V

2.2. Current Starve Ring Oscillator with NMOS Body Biasing

Fig4 present a 3 Stage current starved topology of ring oscillator with substrates of NMOS have been connected to dc supply which is kept at optimum value 0.5V, Vctrl is varied in the range of 0-1V. NMOS substrate bias technique with VCO enhance the oscillation frequency [12, 13]. A positive voltage at the body of NMOS, results on reduction in threshold voltage which leads to high power consumption of the circuit. So it is desirable to choose the optimum value of Vctrl.

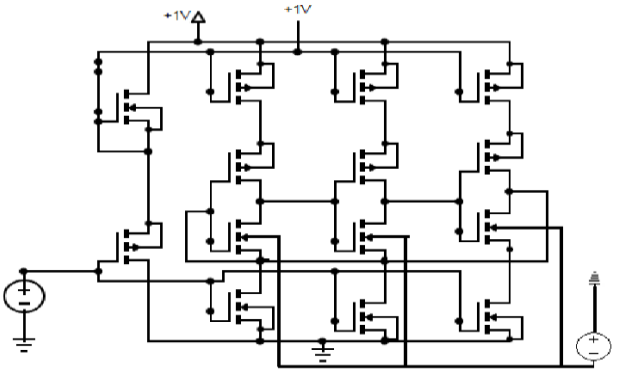

Fig.4. Current Starved ring oscillator with PMOS body biasing

Increasing the body voltage there is increase in the On current up to V_{SB}=0.5 V; further increase in the body voltage decrease the value of I_{DS}. Fig5 shows variation of frequency w.r.t Vctrl keeping body voltage at optimum value 0.5V. Current starve VCO with PMOS Body bias increases frequency proportionally 0.5 to 12.5GHz with control voltage ranges from 0 to 1V. Power consumption of NMOS body biased current starve VCO is drastically increases with increases in oscillation frequency. For frequency 12.5GHz power consumption increases up to 250uW.

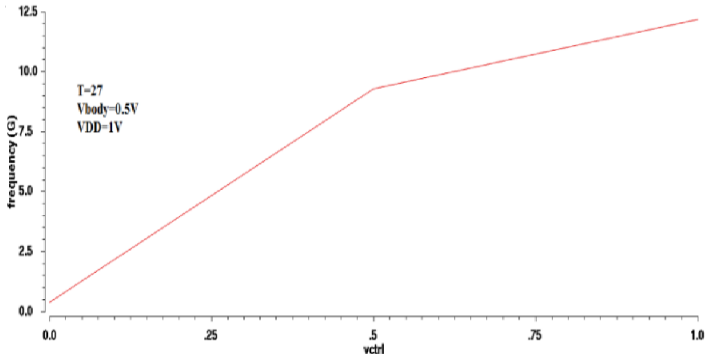

Fig.5. Frequency Variation with Vctrl at body voltage 0.5V

2.3. Adaptive Body Bias Ring Oscillators

Adaptive Body Biasing Ring oscillator is the technique of utilizing the transistor body effect to change transistor threshold voltage during operation by applying adaptive body bias either in forward bias or reverse bias. In this design different body voltages at different Instant of time can be applied which targets to overall wider tuning range of circuit with high frequency along with optimum power saving and phase noise. A fine or

wider tuning range of frequency is major achievement of this work. The bulk terminal of the oscillator is controlled appropriately depending on the required specifications of the circuit. Objective of adaptive body biasing is to maintain the transistor threshold voltage to retain the device performance by applying either forward body biasing or reverse body biasing. Fig6 presents a current starve ring oscillator with adaptive body bias (ABB) network, ABB can be implemented using multiplexer, select lines S0 and S1; it generates a dc output voltage which bias the body of MOS devices in oscillator circuit. Output obtained from ABB circuit is mentioned in table1. The output voltage level obtained from this circuit maintains bulk of MOS more positive or more negative. The performance of the oscillator is maintained in terms of current driving capability by applying either forward adaptive body biasing or reverse adaptive body biasing. Table1 presents 4 different voltage levels generated by ABB circuit; Oscillation frequency (12.54 to 12.62GHz) is unaffected from ABB network. Power consumption greatly decreased from 749uw to 197uw while bulk supply ranges from 0.745V to 66.4uV attainable amplitude of the designed ring oscillator's frequency is 0. 935V for 1V supply voltage.

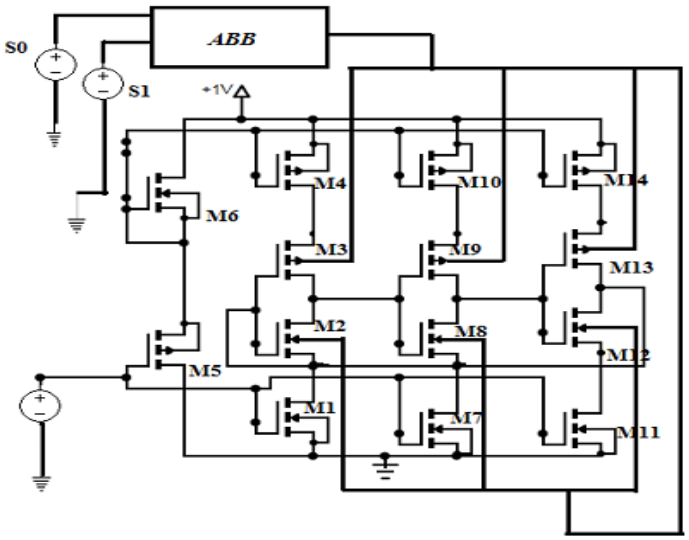

Fig.6. Ring Oscillator with PMOS and NMOS Bulk Connected to Adaptive Body Bias

Table.1. ABB Ring Oscillator at Different Input Level

S0	S1	Voltage Level (v)	Frequency (GHz)	Power (uW)	Phase Noise (dB/Hz)
0	0	0.745	12.62	74.9	-58.1
0	1	0.5	12.56	132	-58.11
1	0	0.24	12.59	112	-58.11
1	1	66.4u	12.54	197	-58.11

Oscillation frequency can further enhance by varying width of transistor, dimensions of transistor depend upon the design speciation of the oscillator, the width of inverter transistors (M4, M10, M14 at 30um) (M1, M7, M11 at 10um) (M2, M8, M12 at 120nm) (M3, M9, M13 at 240nm) the highest possible frequency achievable from this circuit is 13.7 GHz. Fig7 shows the variation in the frequency of the oscillator with width of transistor.

This range of frequency lies to Ku band (Kurtz-Under band) primary used for satellite communication focuses on editing and broadcasting the frequency range of this band lies in 12GHz to18 GHz. Variation in the Channel length results in drastic reduction in frequency by increasing the value of length, so it is advisable to avoid variations with length of MOS. Adaptive body bias circuit with 3 stage current starved ring oscillator present phase noise -58.11db/Hz. Further improvement in phase noise is possible by varying width of MOS. Phase noise varies exponentially with respect to W ratio shown in fig8 with increase in W ratio of transistor, phase noise effect is better which is always desirable.

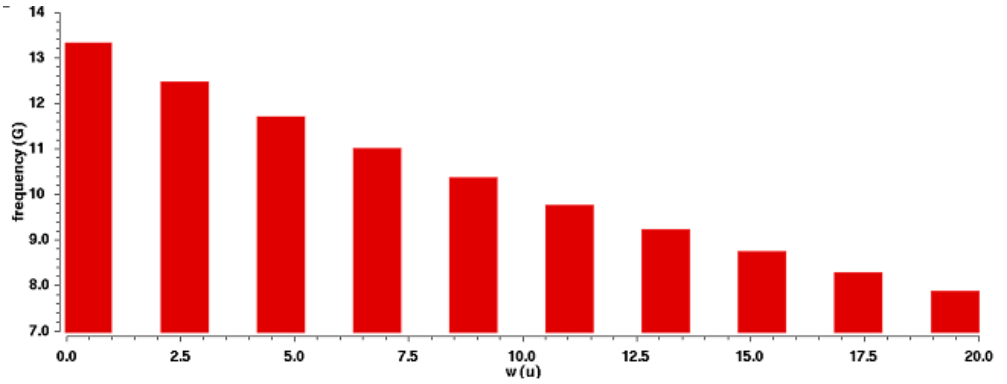

Fig7. Variation of Frequency with respect to W/L Ratio of ABB Ring Oscillator

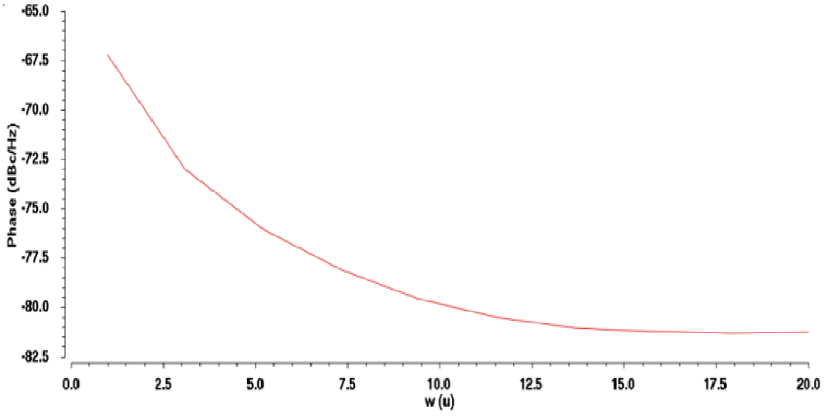

Fig.8. Phase Noise of ABB CS oscillator vs W/L ratio

Table.2. Comparative study of Ring Oscillator with Body Bias

			Operating Frequency with body boas 0.5v				Power				
Reference	Process	Type	Without Bias	PMOS Reverse Bias	NMOS Reverse Bias	Adaptive Bias	Without Bias	PMOS Reverse Bias	NMOS Reverse Bias	Adaptive Bias	Phase Noise (dB/Hz)
[7]	CMOS180nm	Ring	0.958 G - 4.46G				0.226 u				-94.51
[13]	CMOS45nm	Ring		5.33 G	3.8 G	4.76 G		2.68 u	5.68 u	12.03 n	
[15]	CMOS45nm	Ring	5.63 G				10.15 u				-6400
This Work	CMOS90nm	Current Starve	0.626 G	0.5 G - 10.1 G	0.5 G - 12.5 G	10.063G - 10.066 G	490 u	30u	250 u	2.21 m	-60

3. Conclusion

A Body biasing is alternative method to increase the oscillation frequency of ring oscillator. A 3 stage current starve VCO without body bias can have oscillation frequency only 626MHz suitable for L-band application; reverse biasing the PMOS bulk terminal can achieve the oscillation frequency is 500MHz-10.01GHz for control voltage 0-1V while NMOS biasing the achieved results are 500MHz-12.5GHz suitable for Ku band application. Table2 summarized the performance of ring oscillator with either PMOS or NMOS bulk terminal are reverse biased. Adaptive body bias network provides bias voltage for body terminal allow the user to switch reverse bias. PMOS body bias result in less power dissipation compare to NMOS, adaptive bias network yield sustains high oscillation frequency.

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Abhishek Kumar pursuing PhD in Electronics and Electrical Engineering from Lovely Professional University, Punjab, India His area of interest is secured hardware design for random number and secret key, additional silicon IC based feature included in cryptographic module. He is focused on CMOS circuit design for low power, data converter, memory unit and computational circuit at CMOS 90nm technology.

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