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An Insight into Beyond CMOS Next Generation Computing using Quantum-dot Cellular Automata Nanotechnology

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Abstract

CMOS is a technology that has revolutionized the field of electronics. Over the time the processing technologies and design methodologies of CMOS devices have proved to be in full swing with the Moore's law and the miniaturization paradigm. However, after surviving for more than five decades, CMOS is now facing challenges to live through the submicron ranges. The scaling in CMOS has reached a higher limit, showing adverse effects not only from physical and technological point of view but also from material and economical perspective. This drift inspires the researchers to look for new promising alternatives to CMOS which vow better performance, density and power consumption. One of the promising alternatives to digital designing in CMOS is the Quantum-dot Cellular Automata (QCA). QCA is a technology that involves no current transfer but works on electronic interaction between the cells. The QCA cell basically consists of quantum dots separated by certain distance and the entire transmission of information occurs via the interaction between the electrons localized in these quantum dots. In this paper the limitations to CMOS in submicron range and concepts for designing in QCA have been discussed. Further the building blocks are explained theoretically as well as using QCA Designer implementations with focus on cell interaction and clocking mechanisms.

Index Terms: QCA, Quantum Dots, Quantum Cell, CMOS, Scaling, Clocking, Nanotechnology.

1. Introduction

The ever improving life of human beings is the direct result of the advancing technologies that are developed

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from time to time. One of the most important contribution towards the improvement of human life is the development of the field of electronics which has by and large given a new scope to it. The major revolution that forms the core of the electronics industry today is the development of the CMOS technology. This technology has given a new dimension to computing over the last five decades. From 1947, when the first bipolar junction transistors were invented to the time when MOSFET's took over the improvements were occurring at a pace that was not so fast. However after the development of CMOS, the paradigm of miniaturization has achieved much exhilaration and the scaling of CMOS completely met and satisfied this framework. The exceptional growth that the industry has seen over the last few decades has been due to the successful linear scaling which was proposed by Dennard et.al [7], in the basic MOS structure. The scaling of the basic device can be divided into two categories viz. the constant voltage scaling, in which the not so practical concept of scaling of voltage is taken into consideration and the constant field scaling, in which all the dimensions including the power supply voltages and the terminal voltages of the MOSFET are reduced by a same factor. Howbeit it was Moore, who in his paper [4] suggested that the number of components per integrated circuit would approximately double every two years without the corresponding increase in the cost of the chip. This meant that the growth would be exponential. From the time this was predicted by Moore, till today the industry has managed to keep up with the above fundamental famously known as the Moore's Law. However as suggested by the International Technology and Roadmap for Semiconductors ITRS, the CMOS technology has now started to face asperities in maintaining the miniaturization criterion and holding on to the Moore's law [1-3]. The immediate effect of the exponential growth is the ever increasing power dissipation on a single integrated circuit. As the number of components keeps on increasing the power dissipation goes on increasing given a constant power handling capability of the chip. The possibility of removing this generated heat from the chip becomes more and more difficult as the size of the devices goes down to the sub-micron ranges. This implies that the scaling of the basic MOS structure is now reaching the quantum limitations wherein the possibility of further scaling has started to lose its grounds. This is because of the size limitation which means that as the dimensions of the basic device are now approaching the atomic and molecular sizes the possibility of further scaling of the basic device is ruled out leaving no scope for downsizing of the devices [5, 6].

2. Limitations of CMOS Technology

The basic MOS structure, as shown in the figure 1, is a device that consists of metal, oxide and semiconductor, as suggested by the name itself. The semiconductor in the MOS device forms the substrate for the device action, the oxide usually is a dielectric which separates the substrate and the gate and the metal is the electrodes that form the gate, source and the drain.

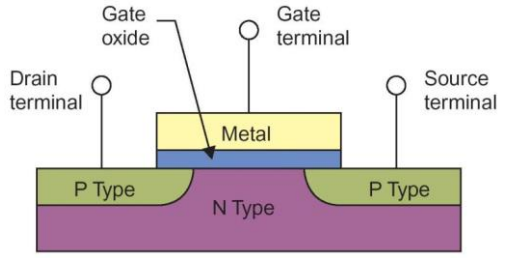


Fig.1. Basic MOSFET Structure

For the required transistor action in this device, substrate and the source, drain are doped with the opposite types of materials resulting in the formation of the opposite polarity channel with respect to the body. This

structure forms the basic MOS device. The basic parameters that determine the characteristics of the device include the voltage applied to the gate terminal called as the gate-source voltage, the voltage between the drain and the source called the drain source voltage, the capacitance offered by the oxide that is the oxide capacitance, the threshold voltage that is the minimum required voltage for formation of the channel and the current that flows between the source and the drain defined as the drain-source current.

As the dimensions of the device are scaled down to the nano meter regime, the parameters are affected by the various quantum effects which results in the degradation in the performance or even the failure of the device. The limitations that the technology is facing does not include a single dimension but has to be envisaged from multiple viewpoints which include the physical, technological, economic and the material perspectives [8]. When we consider the scaling effects, the first and the foremost is the physical effect of this scaling. As all the dimensions of the device are scaled by the same factor both channel length and thickness of the dielectric change. Due to the reduction in the length of the channel the various short channel effects come into the picture. They include the drain induced barrier lowering (DIBL) wherein the high reverse bias at the drain reduces the barrier faced by the carriers and allow the currents to flow for voltages less than the threshold voltage of the device [9]. On the other hand as the scaling diminishes the oxide thickness, it approaches to the width of just a few layers of molecules. Under these size considerations, the various quantum effects start dominating and the electrons start tunnelling through the oxide. Due to this the carriers become available for the voltages at which a normally operated device would not allow conduction. Besides these effects, the short channel of the device can also lead to merging of the source and the drain regions due to the reverse bias of the drain, thereby hampering the basic functioning of the device. To avoid these effects, the doping of the channel can be increased but that again shows adverse effects like the decrease in the mobility of the carriers and the band to band tunnelling. So the physical dimension forms the first aspect into which the limitations of CMOS are rooted.

Apart from the physical aspect, the material stance also plays an important part in not favoring the future scaling. Switching from one material to other in CMOS has not been much of interest to the researchers but now as the end of the technology roadmap is approaching the plunge into the ocean of materials to find a suitable case for CMOS can act as a savior. The technological perspective for the current devices has its life in the various lithographic techniques invented from time to time. However in the deca nanometer regime the conventional lithographic techniques can no longer cope up. So new technologies need to be investigated to give some more life to CMOS. The last but not the least is the economic outlook. The industry cannot go on without actually checking the cost to benefit ratios. We cannot design the components and devices with no returns. Besides, smaller the size more are the defects and the cost of overcoming them. So all these areas need to be studied in order to come up with some solutions to actually implement the concept of "more than moore" today [10, 11].

3. Upcoming Alternates to CMOS Technology

In order to continue with the miniaturization attribute, researches have pointed out two broad categories which include firstly, the development of the CMOS based devices that extend to 3D or vertical dimension and improving material technology etc. and secondly, the switching from the usual transistor paradigm to other phenomena of physics. In order to go with the first option new materials like strained Si or high K dielectrics and new structures like the multi-gate and SOI need to be studied to the extend where they can be used to replace the existing designs in a reasonable amount of time. On the other hand a shift from the transistor based paradigm is the new broad area of research that has been unfolded. It includes a number of alternatives such as the quantum computing, carbon nanotubes, resonant tunnelling devices, single electron devices and the Quantum-dot Cellular Automata Nanotechnology. All these emerging fields are attracting a lot of attention of the researchers since the life of CMOS somehow is to come to an end in a few decades. To obtain if not an alternative, a complement for CMOS, these areas and technologies have witnessed a huge research interest in

recent years [12-13].

4. Quantum-dot Cellular Automata (QCA)

One of the most promising technology as seen by the researchers is the nanotechnology based Quantum Cellular Automata [14]. This technology incorporates a shift from the conventional transistorized designs to designing using nano structures like quantum dots or metal islands. This archetype works on the principles of quantum physics and uses the effects that were a threat to CMOS to its advantage. This is a cellular type of a design as suggested by Von Neumann in his architectures. It was developed by C.S.Lent [14]. The basic QCA cell consists of four potential wells which can be made from quantum dots, metal islands or other nano structures, as shown in figure 2. These wells localize two electrons which tunnel between these due to the presence of tunnel junctions. This quantum mechanical tunnelling forms the first basic principle of QCA designing. The second principle is the most famous law of physics which is the coulomb's law. The electrons in the wells experience a coulombic repulsion between them due to which the electrons in the square structure of the cell take up only two types of stable configurations. These configurations are called as the two types of polarizations of the cell, as shown in figure 2. They represent the binary zero and binary one for the digital designing using QCA. However in the QCA cells no tunnelling is allowed between the adjacent cells and hence there is no current flow in this technology. Here the interaction between the cells forms the basic mechanism of functioning. The cells which are adjacent to each other have the ability to effect the polarization of each other. Due to this the state of each cell depends on the state of the adjacent cell.

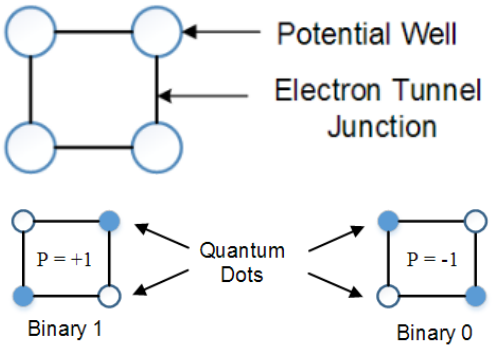
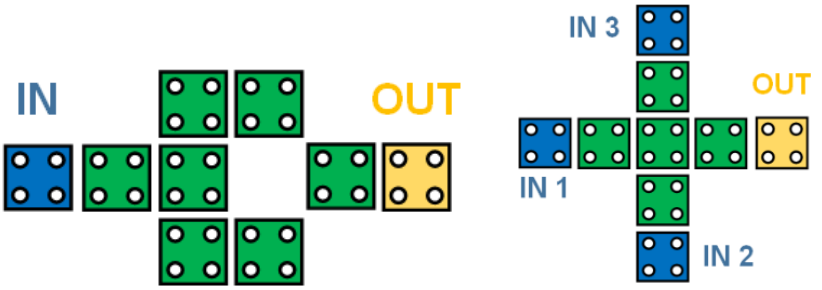


Fig.2. A basic QCA cell and Binary 1 and 0 polarization representations.

The QCA designing follows the phenomena of processing in the wire and memory in motion which means that the interconnections in this technology are not different from the circuits used [21,31,32]. The cell which is provided with the input effects the cell next to it and changes its polarization so as to achieve a stable state with least coulombic repulsions between them. In this way long wires called as binary wires can be designed in QCA. The majority gate and inverter form the other two most important components in QCA. All these components are shown in the figure 3.

(a)

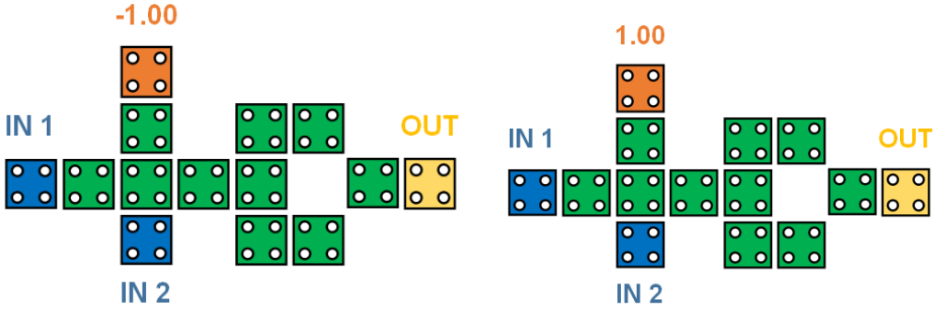


(b) (c)

Fig.3. (a) Binary Wire, (b) Inverter and (c) 3-Input Majority Gate in QCA

The inverter is designed using the 45° cell at the corner in the design. Due to this shift of the cell, the least coulombic forces are experienced in the cell alignment with opposite polarization and hence an inverter. The majority gate, as the name suggests achieves a stable state depending on the value of the three inputs. In this gate the central cell called as the device cell takes up the polarization of the majority of inputs to achieve a stable state [15-16]. Just as in digital logic we have some basic circuits from which the entire digital circuitry can be designed, in QCA. Besides the design of basic Boolean functions the entire circuitry of a digital computer can be designed in QCA. For example, by fixing one of the input of the majority gate to zero, an OR gate can be designed. Similarly by fixing one input to one, an AND gate can be realized.

By combining these AND and OR gates with the inverter NAND and NOR logics can be achieved. Further by proper connections between the majority gates other Boolean functions can be realized. The basic designs of NAND and NOR gates are shown in figure 4.



(a) (b)

Fig.4. (a) NAND and (b) NOR Gate Implementation in QCA

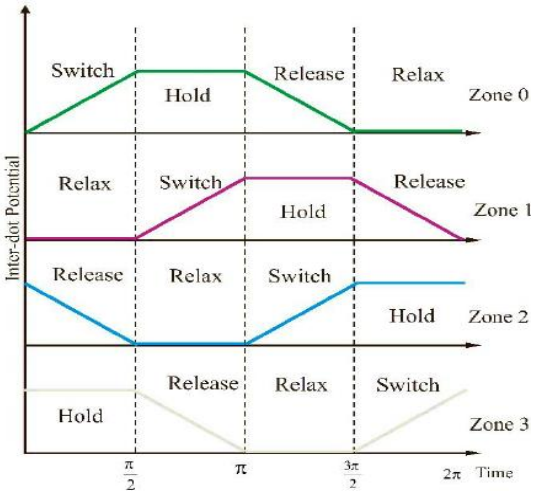
The basic method of designing involves the conventional majority voter designing. Other than this a number of design methodologies have been suggested one of which is the designing based on the explicit interaction of cells [25,31,32] and the other is the tile based designs. All these designing methods are under research and a break through from these is expected, thus leading to the revolution from the transistor based designing to the no current paradigms. Some of the designs in QCA are discussed in the next section.

The proper flow of information in the QCA architectures is ensured by the clocking of the circuits which is provided by the underlining CMOS or carbon nanotube wires. The function of this clocking is to provide the electric field to the QCA cells which in turn controls the raising and lowering of the barriers between the wells. Due to the change in the barrier potential, the electrons in the wells are either localized or allowed to tunnel to

other well. If the barriers are lowered, the electrons tunnel from one well to another such that to ensure least coulombic repulsion with respect to the adjacent cells. On the other hand, if the barriers are raised, the electrons localize in a particular well and the tunnel junctions are closed to any movement of electrons. In QCA, one clock cycle consists of four phases. The phases decide whether the barriers are low or high. The first is the switch phase, in which the barriers are lowered and the electrons are allowed to respond to the effect of the adjacent cell. By the end of the switch phase, the electrons take up a particular polarization corresponding to the neighboring cell. The next phase is the hold phase, in which the barriers are raised and no movement of electrons occurs. In this case the cell is in the position to influence the adjacent cell. Depending on the clock phase of the next cell it may either remain in the same state (if this is also in hold state) or change its polarization (if it is in switch or release phase). The phase that follows the hold phase is the release and relax phase in which the barriers are again lowered and the cell again attains the null polarization. For proper working of the QCA circuits the clocking of the circuits in a proper manner is very important. The clock phases should follow each other in a proper manner otherwise the information flow can be distorted. Due to four phases, the QCA architecture is provided with four clock zones as shown the figure 5. The proper flow of information is also explained in figure 5. In QCA the different phases of a clock cycle are represented by different colors [29-31].

5. QCA Based Digital Design Implementations

In this section some basic designs in QCA have been discussed to get an idea about the flow of information via pipelining. As discussed earlier the binary wire, inverter and the majority gate form the basic building blocks in QCA. All the circuitry designed using QCA involves the use of these basic building block. We have already discussed the designs of basic Boolean functions. The digital circuitry however comprises of two broad categories of designs which are the combinational and the sequential logic. In conventional digital designing the clock is required only in sequential logic whereas in case of QCA designing clocking is required in both combinational and sequential logic designs [17-19,27,28,31]. The optimization parameters in this technology include the cell count of the design, latency, cell area, total area and complexity of the design. Here we have discussed some of the widely used combinational and sequential circuit designs and have also explained the basic working and clocking of the designs.



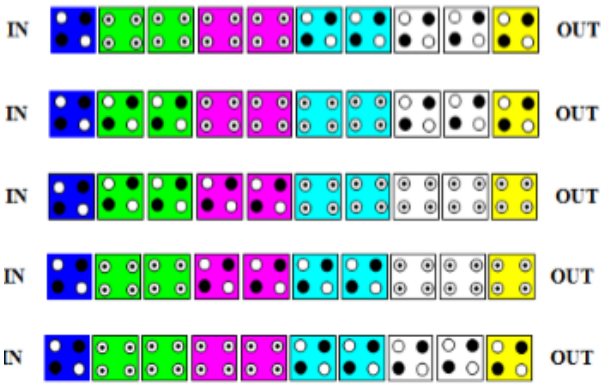


Fig.5. Clocking Zones and Phases Along with Illustration of Information Flow in QCA

The figure 6 shows the QCA implementation of a half adder along with the simulation results that have been achieved in the QCA Designer 2.0.3. From the equations of the half adder we know that we have a sum and a carry output, given by the equations $Sum = A \oplus B$ and $Carry = AB$. So we now need to implement these two equations in order to design a half adder in QCA. The majority equations can be written in order to simplify the design process. The majority equations for a half adder are given by

$$SUM = M(M(A, B', -1), M(A', B, -1), 1) \tag{1}$$

$$CARRY = M(A, B, -1) \tag{2}$$

From the carry equation we see that it simply consists of a single majority gate in which one input is fixed to one in order to obtain an AND operation. The equation for sum is however more complicated as it involves the designing of an Exclusive-OR gate. The equation of the Exclusive-OR function is given by $A'B \oplus AB'$. This means that the implementation of the Ex-OR function needs two inverters, two AND gates and one OR gate. This is implemented in the figure 6.

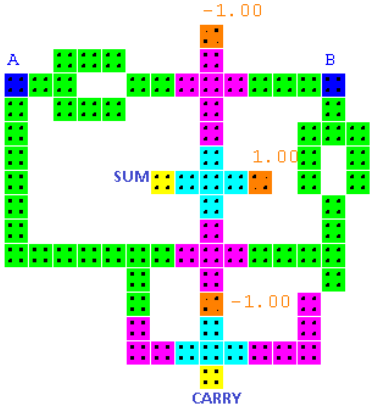


Fig.6. QCA Implementation of a Half Adder

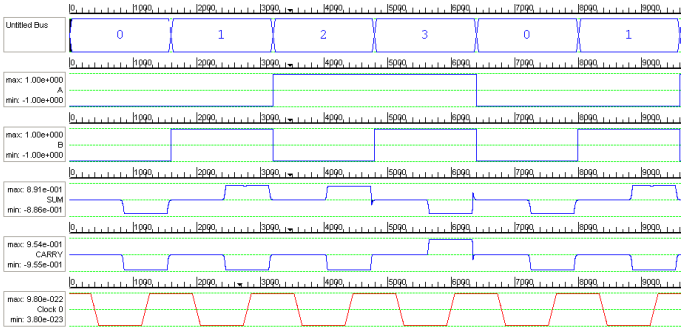


Fig.7. Simulation Result of a Half Adder using QCA Designer 2.0.3

The other circuit is the full adder. This adder can be designed using the conventional majority voter method but here we have shown the design using the explicit interaction of cells. The implementation full adder in QCA Designer 2.0.3 is shown in figure 8.

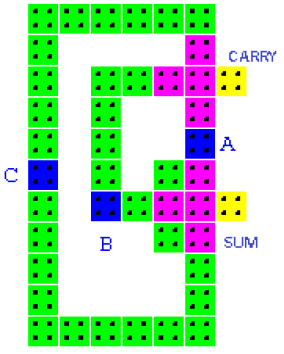


Fig.8. QCA implementation of a full adder

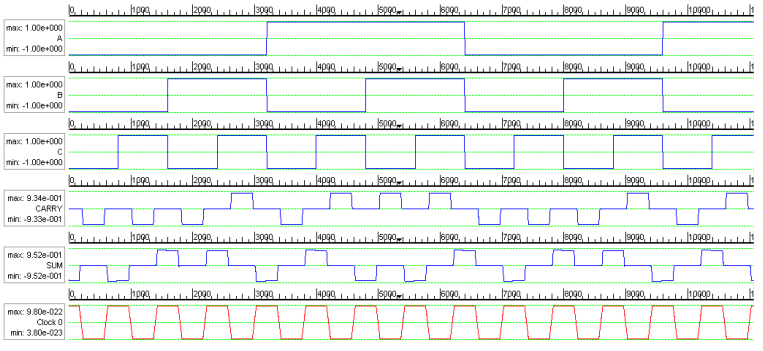


Fig.9. Simulation Results of a full adder using QCA Designer 2.0.3

The sequential circuits are the other class of digital circuits which are the fundamental in the designing of complex computer architectures [20]. The basic sequential circuit is the flip flop. We have considered a basic D flip flop design. The D flip flop is basically a delay flip flop which means that one D flip flop provides a delay

of one [26]. We also know that in QCA one clock cycle consists of four phases and is equal to one delay. Hence a simple QCA wire which has all four phases of the clock can provide a delay of one and can hence act as a D flip flop. This is shown in figure 10.

Fig.10. QCA Implementation of D-Flip Flop

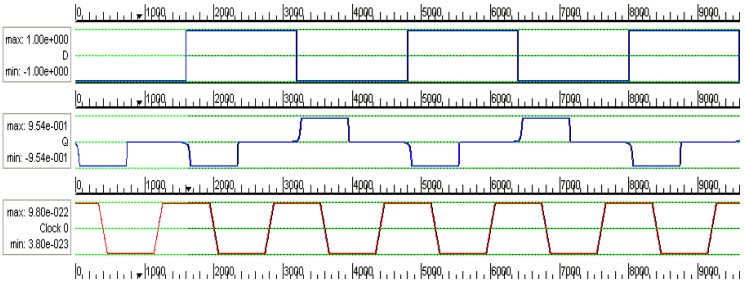


Fig.11. Simulation Results for D-Flip Flop using QCA Designer 2.0.3

The other sequential circuit we have considered is the four bit shift register. It consists of four D flip flops. After each clock cycle i.e. each D flip flop the bits are shifted. This is shown in figure 12.

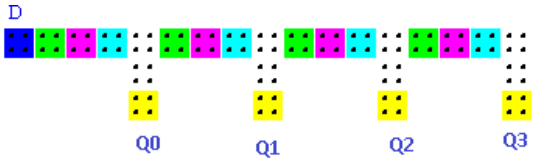


Fig.12. 4 Bit Shift Register Using D Flip Flop

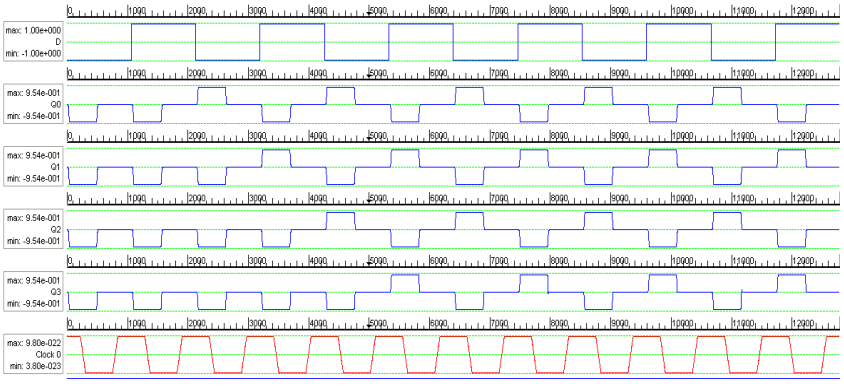


Fig.13. Simulation Results of Shift Register Using QCA Designer 2.0.3

Besides the combinational and sequential designing using QCA, a new emerging digital logic is finding wide scope in design using QCA technology. The logic is called as the reversible logic which suggests that the power is dissipated in the circuits due to the erasing of the bits during computation. This principle was given by Landauer. It suggests that for every bit that is erased KTln2 joules of energy is dissipated. If these computations are somehow performed in a reversible manner that is without the erasing of the bits the power dissipation can be reduced to a great extent [22-24]. However the design of the reversible circuits has been the greatest challenge faced by the researchers. QCA is suggested as the break through by which these circuits can be implemented. Reversible logic along with QCA technology if accomplished will result in ultra-small devices and ultra-low power dissipation.

6. Advantages of QCA

QCA stands as a strong contender as an alternative or complement to CMOS due to the numerous advantages it offers over the conventional CMOS technology. Some of the important advantages over CMOS involve the ultra-small size designs that are possible using this technology. The basic cell in QCA is only a few nanometers in size and thus the overall architectural area depends on the efficiency of the designs which are implemented. This results in the achievement of very high density circuits in QCA which cannot be possible with the present CMOS structures. QCA technology is an edge driven one which means that the input is to be applied to a single cell at the edge. The inner cells respond to the input cell and adjust their polarization. This also suggests that no power lines are required and the resulting architectures are therefore ultra low power designs. This is the most important advantage of QCA since this power dissipation is the main showstopper for the CMOS technology.

7. Conclusion

In this paper we have reviewed the CMOS technology and have discussed the various limitations that are forcing the CMOS towards the end of the technology roadmap. Further we have envisaged the future of the electronics industry in either improving CMOS materials and structures or shifting from the transistor based paradigms. We have focused on one of the promising upcoming alternative of CMOS which is the Quantum Dot Cellular Automata. We have discussed the basic building block in QCA and the fundamentals of the working of the QCA architectures via clocking and pipelining. The various examples to understand the basic designs are discussed and the advantages of QCA over CMOS are listed. We thus conclude that the shift from the transistor based paradigm may not take years but decades of effort but they are the need of the hour for nanotechnology and next generation computer architectures.

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