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A New Approach for RFID Tag Data Reading in FPGA by using UART and FIFO

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Abstract

Nowadays, Radio Frequency Identification (RFID) technology used for automatic object tracking and identifying purpose. RFID technology used in so many applications especially in automobiles, security and health care systems. RFID reader and RFID tags are main processing units in RFID system. RFID tags give the information on what an object is, where it is and even its condition, and what is happening, share related data and respond to the reader. RFID reader module used for reading data from lots of RFID tags. In convention methods [1][2] doesn't contain any read controller methodology and doesn't contain any storage element for RFID tags data storing. In this paper, we propose a new approach for RFID tag data reading in FPGA. This approach is more flexible in structure and easily updates the design for any applications. This design is easily adaptable for different chips and communication mechanism. This design has reading controlling methodology and along with storing capability of RFID tags by using FIFO. Here we are using Universal Asynchronous Receiver and Transmitter protocol for communicating RFID reader to PC. For simulation, we are using ModelSim software and for synthesis, purpose using XILINX ISE 14.7.

Index Terms: RFID reader, RFID Tag, UART, FIFO, FPGA, VERILOG, ModelSim, XILINX ISE 14.7.

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1. Introduction

Radio Frequency Identification Technology (RFID) is a wireless technology used for automatic object identifying. This technology uses the radio magnetic waves for transferring data between RFID tag and RFID reader. RFID technology is the replacement of a Barcode system and there is no physical contact between the

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Tag and Reader. RFID system mainly contains two processing units [3][4]. They are

- RFID TAG
 - Active Tag
 - Passive Tag

Nomenclature

RFID	Radio Frequency Identification
UART	Universal Asynchronous Receiver and Transmitter
FIFO	First In First Out
UID	Unique Identification Number
FPGA	Field Programmable Gate Array

RFID READER

RFID Tags are attached to the object and that tags tell what an object is, where it is and its condition. RFID tag contains storing element. Storage element contains the object details. RFID tags are classified as the Active tag and Passive Tag. Active Tag contains a battery for transmitting data to the reader. Active Tag is communicated the longer distances but it is costly. A passive tag doesn't contain any battery. RFID Passive Tag active when power is received from RFID reader. Passive tag communicates smaller distance and it is cheaper. A reader sent power source to tag through electromagnetic induction coupling principle. Induction coupling means to transfer the energy from one circuit to another circuit through electromagnetic waves. A RFID tag contains Unique Identification Number (UID) for identifying the object details. This UID number is read by the RFID reader and sends the UID in serial form by using UART. RFID system transfer data between the reader and Tag without any physical contact. Data was transmitted through radio frequency waves. It will operate the radio frequency at low-frequency between 125 kHz-134 KHz and high frequency at 13.56 MHz and Ultra High-frequency range from 860 MHz-960 MHz [4] Fig 1 gives the information on RFID communication system.

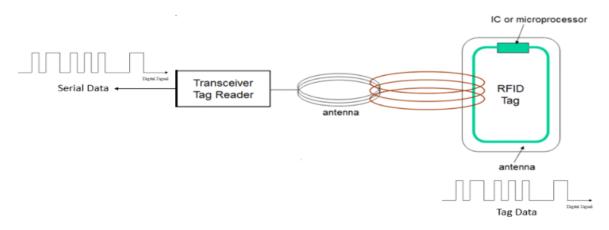


Fig.1. RFID Communication System

2. Previous Approach and Proposed Method

2.1. Existing Method

In convention method approaches [1][2], RFID tag data reading was done by using serial communication and with the help of PC. In this process, there is no read controller module. This process is only for checking RFID tags are working or not and doesn't contain any storage of RFID tags further uses. Fig 2 shows the block diagram of RFID tag reading. In this figure RFID tag data is read by using MFRC500 (RFID reader module) and sends the data to the pc through UART interfacing. This approach is not applicable for storing RFID tag data.

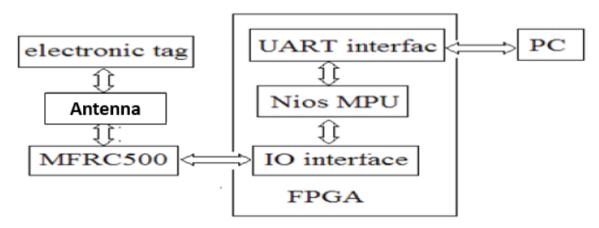


Fig.2. Previous Approach for RFID Tag Data Reading

2.2. Proposed Method

Fig 3 shows the proposed method for RFID tag data reading in FPGA. The proposed method is flexible in the structure and easily adaptable for different chips and communication protocols. This module contains the reader controller module for further development. This module stores RFID tags data by using FIFO (First in First Out). This module can update easily. These module works as follows

- When RFID tag comes near the RFID reader module it will reads the information from the RFID tag.
- Sends the Data in the serial format by using UART communication protocol.
- UART receiver reads the data in serial form sends Byte format to the Data Management module.
- Data Management module checks the received data send data to the write module. This module writes the data into the FIFO.
- FIFO means First In First Out.
- After writing data into the FIFO data will be read by using read controller module.
- UART transmitter module sends the data in the serial form.
- After read controller module we can place any other decoding circuit for application development and any other display monitoring system.

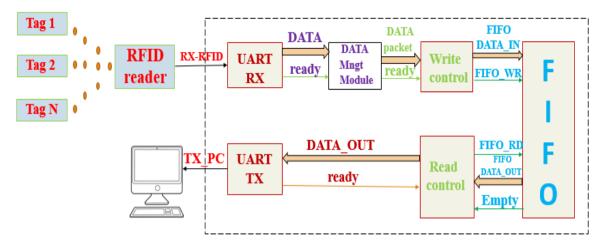


Fig.3. Proposed Block Diagram for RFID Tag Data Reading in FPGA

3. Internal Block Explanation

3.1. Universal Asynchronous Receiver and Transmitter

UART is an Asynchronous communication system that means data will not depend on the clock signal. UART is serial communication and used a single wire for transmitting/receiving data. UART has some standard configuration parameters; they are Baud rate (2400, 4800, 9600...), start bit, data bits, stop bit, a parity bit and flow control. Before going to the communication establishment, we need to fix these parameters as same as in receiver and transmitter. Fig 4 indicates the UART data format. UART contains receiver and transmitter modules. In these design, we are taken configuration parameters as baud rate (9600), data bits (8-bits), a start bit (1-Bit), stop bit (1bit) and no flow control, no parity bit.

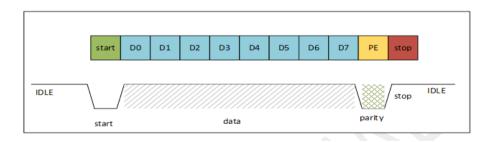


Fig.4. Data Framing

3.1.1. UART Receiver

UART receiver module receives data in the serial form and output in parallel form. In this module, we use simple shift registers for getting parallel data. UART receiver module is designed by using FSM. Data was taken at the middle of samples in the data frame. This module is active when serial data is the active low position. Fig 5 and fig 6 shows the block diagram of UART receiver module and output waveform respectively.

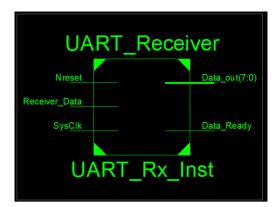


Fig.5. Block Diagram of UART Receiver module

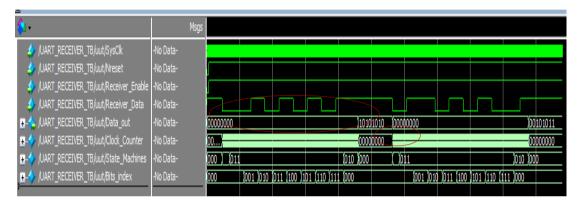


Fig.6. Output waveform of UART Receiver

3.1.2. UART Transmitter

UART transmitter module works same as the shift register. UART transmitter module design follows same as the UART receiver module. In this module, data will be shifted serially. Fig 7 and Fig 8 shows the block diagram of UART transmitter and output waveform. These module receives the data in the form of parallel and sends data into the serial.

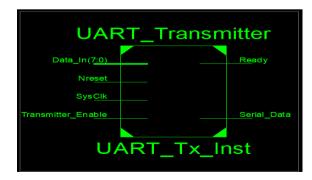


Fig.7. Block Diagram of UART Transmitter Module

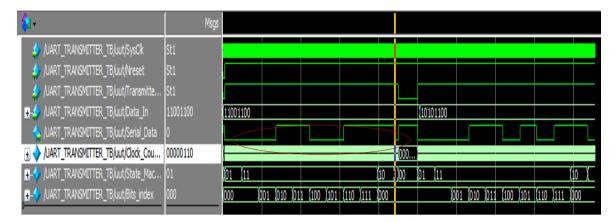


Fig.8. Output waveform of UART Transmitter

3.2. Internal Module

3.2.1. Data Management System

UART receiver module outputs are connected to the Data Management System module. This module receives the parallel data from the UART receiver module. This module taken Byte data from UART receiver module and checks received data correct or not. This module checks the start byte (0x0A) of RFID tag and stops byte (0x0D) of RFID tag. If the start and stop byte is correct then RFID tag data packet sent to the write controller module. Data Management System module using simple shift registers, comparators. Outputs of Data Management System module is connected to the write controller module. Fig 9 and Fig 10 gives the block diagram of data management module and output waveform respectively.

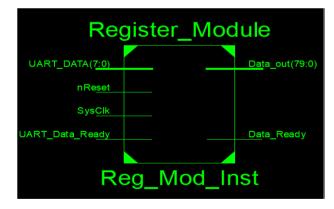


Fig.9. Block Diagram of Data Management Module

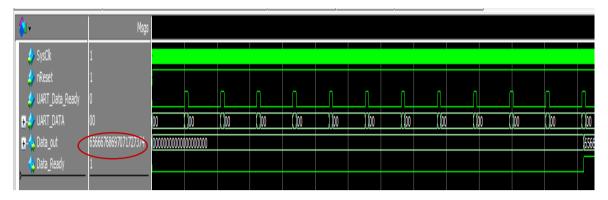


Fig.10. Output waveform of Data Management Module

3.2.2. Write Controller

Write controller module is used for writing data into the FIFO. When Ready goes high it will read RFID data packet and send 8bit data every 3 clock signals and sends write signal on second clock signal due to this data will stable when writing happens into the FIFO. Fig 11 indicates the block diagram of write controller module. Fig 12 shows the data written into the FIFO.

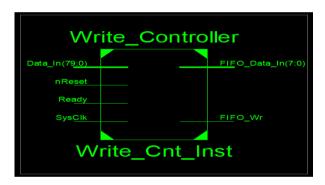


Fig.11. Block Diagram of Write Controller Module

*	Msgs											
🁍 SysClk	1	M	MM	່ເກມ	M	M	บ	M	M	hnn	Innn	ЛЛ
👍 nReset	1											
🖃 🎝 Data_In	65666768697071727374	000000000000000000000000000000000000000	00000	656667	68697071	727374						
👍 Ready	0											
📕 👍 FIFO_Data_In	74	00		65	66	67	68	69	70 71	72 7	3 74	
👍 FIFO_Wr	0			Ĺſ	1							
·····												

Fig.12. Data is Written into the FIFO

3.2.3. READ CONTROLLER

Read controller sends the read signal to the FIFO and reads the data from the FIFO. Read controller module sends Byte data to the UART transmitter module. This module also receives a ready signal from UART transmitter module for indicating data is transmitted in the serial form. This module also makes an important role in RFID tag reading. This module active when FIFO contains any data. By using this module we can develop any application. For developing application require UID number. These numbers stored in the FIFO and these data read by using read controller module. Fig 13 and 14 indicates the block diagram and the output waveform of reading controller module respectively.

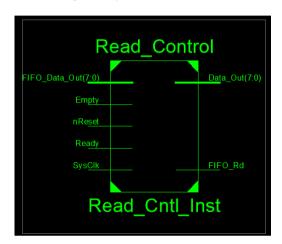


Fig.13. Block Diagram of Reading Controller Module

V	Msgs										
🍐 SysClk	St1										
ᄼ nReset	St1										
₽ FIFO_Data_Out	bb	aa)bb				
约 Empty	St1										
👍 Ready	St1										
🖕 FIFO_Rd	StO										
📕 🔶 Data_Out	bb	00			3 a			b	b		
P											

Fig.14. Output waveform of Reading Controller Module

4. Experimental Results

RFID reader reads the information from RFID tag through radio frequency waves and reader will send the data in serial form. RFID reader sends start byte (0x0A), data bytes (10 Bytes) and stop byte (0x0D) respectively. Fig 15 indicates the RTL schematic view of the proposed method. Fig 16 shows the data receiving from RFID reader in serial form.

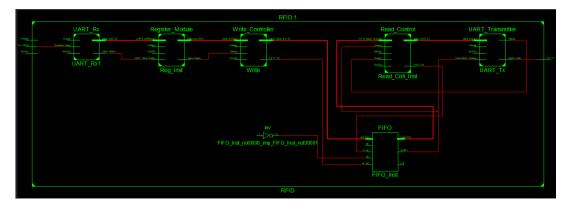


Fig.15. Rtl Schematic of Proposed Method

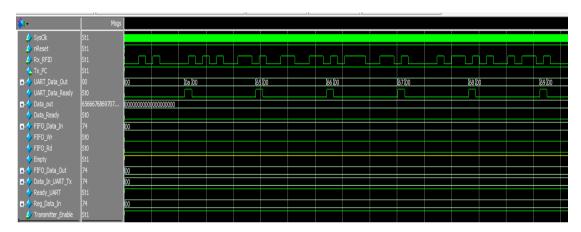


Fig.16. Reading the Information from RFID Tag

UART Receiver receives data in serial and sends in byte format. Data management system checks receiving correct data or not and sends a data packet to the write controller module. This module writes the byte data into FIFO. Fig 17 shows the write data into the FIFO.

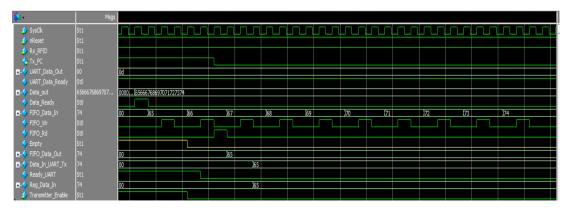
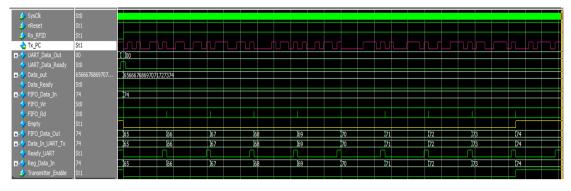


Fig.17. Writing Data into the FIFO by Write Controller

Read controller module reads the data from FIFO and sends to UART transmitter module. This module receives data in the parallel form and sends in serial form. Fig 18 shows the sends data in serial form by UART Transmitter.



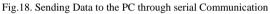


Table 1. Difference between Existing Method and the Proposed Method

Parameters	Existing Method	Proposed method		
Adaptable for Different communications	YES	YES		
Adaptable for different Chips	YES	YES		
Update available	YES	YES		
Storage capability	NO	YES		
Read Controller	NO	YES		
Application development	NOT POSSIBLE	POSSIBLE		
IP-core generation	NO	YES		

With the help of Hyper Terminal, we can see the RFID tag data. Table 1 gives information difference between existing method and the proposed method. The proposed method is applicable for application development and fig 19 shows the development of IP core. Table 2 shows the experimental results of the proposed method and executed in the Xilinx ISE 14.7. Maximum PATH DELAY: 2.184ns

omponent Library	393	enrcon	ents Address Ma	p Clock Settings Project Setting	gs Instance Parameters System Ins	pector HDL Example Generation					
×	- 🔶	Use	Connections	Name	Description	Export	Clock	Base	End	IRQ	Opcode Na
Project	X			Cik 0	Clock Source						
New Component				ck_in	Clock Input	clk					
RED READ	1.1		<u>ې</u>	clk_in_reset	Reset Input	reset					
Library	X			clk	Clock Output	Double-click to export	clk_0				
Onfig-Bypass App Example				clk_reset	Reset Output	Double-click to export					
Bridges				nios2_qsys_0	Nios II Processor						
Bridges and Adapters	1.1		•	→ clk	Clock Input		clk_0				
Clock and Reset	Z		• •	→ reset_n	Reset Input		[clk]				
Configuration & Programming	8			data_master	Avalon Memory Mapped Master		[clk]	IRQ	0 IRQ 3:	ι κη	
0.0SP				— instruction_master	Avalon Memory Mapped Master		[clk]				
Embedded Processors			$ \succ$	jtag_debug_module_re.			[clk]				
Interface Protocols				→ jtag_debug_module	Avalon Memory Mapped Slave		[clk]		Ox8fff		
Memories and Memory Controllers			×	— custom_instruction_m	Custom Instruction Master	Double-click to export					
Merlin Components				onchip_memory2_0	On-Chip Memory (RAM or ROM)						
Microcontroller Peripherals			•	→ clk1	Clock Input		clk_0				
Peripherals			•	→ s1	Avaion Memory Mapped Slave		[clk1]	= 0x0000	0x7fff		
P-PLL			• •	→ reset1	Reset Input	Double-click to export	[clk1]				
- Qsys Interconnect				jtag_uart_0	JTAG UART						
Verification			•	→ ck	Clock Input		clk_0				
Window Bridge			• •	→ reset	Reset Input		[clk]			11	
			••	→ avalon_itag_slave	Avaion Memory Mapped Slave	Double-click to export	[clk]		0x9007	≻—0	
				FID_READ_0	RFID_READ						
			•	→ clock_sink	Clock Input		clk_0				
			• • •	→ reset_sink	Reset Input		[clock_sink]				
				conduit end	Conduit	rfid_read_0_conduit_end					

Fig.19. IP core Generation for RFID Tag Reading

Table 2. Simulations Results of Proposed Method

Device Utilization Summary (estimated values)											
Logic Utilization	Used	Available	Utilization								
Number of Slices	316	4656	6%								
Number of Slice Flip Flops	418	9312	4%								
Number of 4 input LUTs	375	9312	4%								
Number of bonded IOBs	4	232	1%								
Number of BRAMs	1	20	5%								
Number of GCLKs	1	24	4%								

5. Conclusion

In previous approaches, RFID tag data reading was done by using serial communication and with the help of PC. In previous approaches, there is no read controller module. Previous process is only for checking RFID tags are working or not and doesn't contain any storage of RFID tags further uses. Proposed method is flexible in the structure and easily adaptable for different chips and communication protocols. This module contains the reader controller module for further development. This module stores RFID tags data by using FIFO (First in First Out). This module can update easily. This module also useful for application development process.

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