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A Low Power Consumption Architecture Model for Multiple Processors on Optical Printed Circuit Board

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Abstract

Traditional single-core processors and multiprocessors architectures encounter some problems which are high heat generation, high cost to produce and high power consumption. In this paper, a model to achieve low power consumption by using several processors managed separately with useful energy saving strategies including switching the mode of processors, assign tasks to different CPUs, using optical fiber as transmitting media etc. is proposed. In this way, the architecture manages to disperse the energy dissipation. Some evaluations on power consumption, cost and performance are made which proves that it is an effective method to reduce the power consumption.

Index Terms: optical interconnection; computer architecture; low power consumption; multiple processors

1. Introduction

Traditional single core processors enjoyed a blooming period in the past four decades. In order to achieve a low power consumption, former designers tend to lower the voltage and smaller the size of chip. It is well recognized that processor clock frequency is the main concern factor of system performance. However, it becomes more and more difficult for us to raise the single core processor clock frequency because the cost to decrease the size of the chip is becoming higher and higher and the time to design and conform a new single core processor becomes longer and longer [1,2]. Thus, Chip Multiprocessor (CMP) organization becomes popular. CMP architecture which uses several simple processors organized in some key technology such as cache coherent design, kernel interconnection and multi-kernel tasks to some point increases the performance of computers, but heat generation and power consumption are problems that cannot be overlooked [3,4]. Symmetrical Multi-Processing (SMP) technology, one kind of CMP architecture, uses two or more identical processors are connected to a single shared main memory and are controlled by a single Operating System (OS)

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instance. The SMP systems have a relatively strong advantage in distribute computing which means the performance of SMP systems are excellent [5]. But the transmit bandwidth limit their development.

In addition, recent optical communication development is significant. The former trend of optical communications prefers to use it in a large scale of area. However, small-scale applications of optical communications become popular and low cost. Mu Hee Cho proposes a method for high-coupling-efficiency optical interconnection. In this way, we can develop optical printed circuit boards [6]. Patrick W. Dowd suggests an approach to improve the performance by using Wavelength Division Multiple Access (WDMA) technology [7]. Further, Biswanath Mukherjee presents the progress and challenges for optical communication networks which means that optical networks is developing at a very high speed [8]. Also, optical communication on board-level overcomes the shortage of heat generation comparing to wire commutation [9]. Hence, using optical fiber as bus media on board is a wise choice.

In order to solve the above mentioned problems, we propose a low power consumption method by organizing several processors on an optical printed circuit board. This paper is organized as follows. Section II describes the whole architecture model. Section III evaluates the model in three different prospective. Finally, Section IV concludes.

2. Architecture model

2.1 Architectural features

The architecture contains a number of processors and several memory and devices.

Several crucial features are as follows.

1) The processors are arranged according to the structure of rectangular solid on the board.
2) One main processor controls the status and power of other processors.
3) Each of the processors is connected to at most one memory.
4) Each processor is connected to and one or a few input/output devices, so devices are controlled by the corresponding processors.
5) Using optical fiber as transmitting media, so the processors can use it to deliver control message or data.

2.2 Nodes

Fig.1 illustrates the overall structure *S* which can be described as

$$S = \{P, M, D\}, \tag{1}$$

where *P* is processors, *M* is memory, and *D* is devices. The device we concerns could be a real physical device, and also could be a virtual device in a software concept way such as file system, a special part of memory etc..

In Fig. 1, the processors can be numbered from 1 to N, where $N \in \{4,6,8,12,20\}$. Also, memory can be numbered as $R(i),\ \ i = 1,2,...,N$ and devices numbered as $D(j),\ \ j = 1,2... .D(j)$ is managed by the specific processor.

To make it more convenient to describe, we define a node as

$$node(n) = \begin{cases} P(n) + M(i), & if\ connected\ to\ a\ memory \\ P(n), & if\ not\ connected\ to\ a\ memory \end{cases}, \tag{2}$$

where $n \le N$ *and* $i \le N$, $P(n)$ is the n^{th} node's processor. If $P(n)$ is connected to a memory, we should add $M(i)$ to make it a node.

The main idea of this architecture is to use different node to control a few number of devices so that when the devices comes to useless, we could control the correspond node to a sleep mode status. Therefore, we can save the energy.

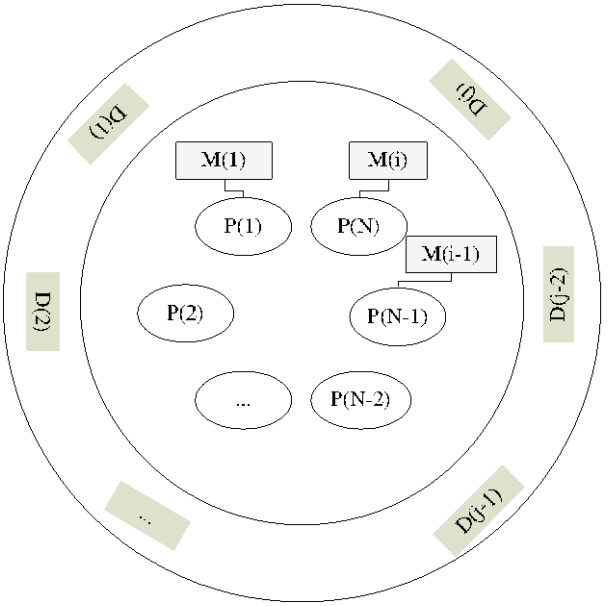

Fig 1. Sketch of system architecture

2.3 Relationship between node and devices

In this architecture, the relationship between nodes and devices are one to one or one to many. It means that one node could control more than one device.

Fig. 2 shows that *node*(1) operates $D(1)$ by opening/closing and any other necessary management while *node*(2) is responsible for opening/closing $D(2)$ and $D(3)$. The rest can be done in the same manner. However, the amount of devices which is managed by the corresponding processor has a great effect on the performance of the proposed architecture, i.e. more devices, less power saving.

Unlike one processor manages all the devices which connected to the computer, the proposed method that managing one or a few number of devices by each processor is used to keep the devices independent.

In order to synchronize clock of the processors, we use a design method based on Euclidean space to arrange the processors. As we all know, there are only 5 rectangular solid which are regular tetrahedron, regular hexahedron, regular octahedron, regular dodecahedron and regular icosahedron in Euclidean space. So we put every node on the vertexes of the rectangular solid. That's why $N \in \{4, 6, 8, 12, 20\}$ .Because of the limit of rectangular solid, only 5 ways of arrangement could be made to build the architecture. However, regular icosahedron which has 20 vertexes will be more than enough to satisfy the modern computers.

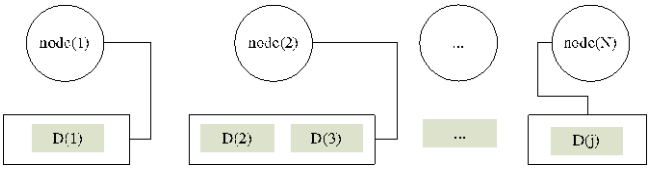

Fig 2. Sketch map of nodes and devices

2.4 Connections

Light is one of the most excellent matters in modern computer architecture design. Thus we use optical fiber as our transmitting media to connect processors, memory and devices.

Additionally, optical fiber has the following characters:.

6) Super high speed. In the optical fiber, optical signal travels at almost light speed.
7) Strong transmits ability. Using optical fiber means that we could get more transmission bandwidth to send and receive more data parallel.
8) Less signal attenuation. Compared to the signal transmits by traditional electric wire, the signal through optical fiber loses less in the whole process of transferring.

Consequently, optical fiber is an ideal choice for our architecture to achieve low-energy-cost and high efficiency.

By using optical printed circuit board (O-PCB) instead of traditional electric printed circuit board, our architecture can be more effective and reliable. At the same time, a number of laboratories (HP Lab etc.) and companies (Intel etc.) are doing researches and experiments on O-PCB products. However, one obvious problem that traditional processors are using copper as the wire must be solved. Thus, we must use a light and electric transformer to do the job to keep the signal going from processor to processor.

2.5 Energy Saving Strategy

To save the energy as much as possible and have a relatively good performance, the following rules are made.

- Two modes (wake-mode and sleep-mode) are available to every single processor.
- One main processor assigns and manages tasks for others.
- Optical printed circuit board instead of electric printed circuit board is used to decrease heat generation and increase transmission efficiency.

3. Evaluation

Fig. 3 shows the power consumption of a computer whose configuration is Intel X58 mainboard, Intel Core 2 dual CPU E8190, ATI Radeon X1650GT, Western Digital hard disk 320G and some other normal devices. The total power consumption is 269 Watts (w).

3.1 Power consumption evaluation

From Fig. 3, we can see that the mainboard, CPU and GPU are three primary energy consumption sources. Suppose we are dealing with four processors architecture by our method. To calculate the total power consumption, we get the formula [10]

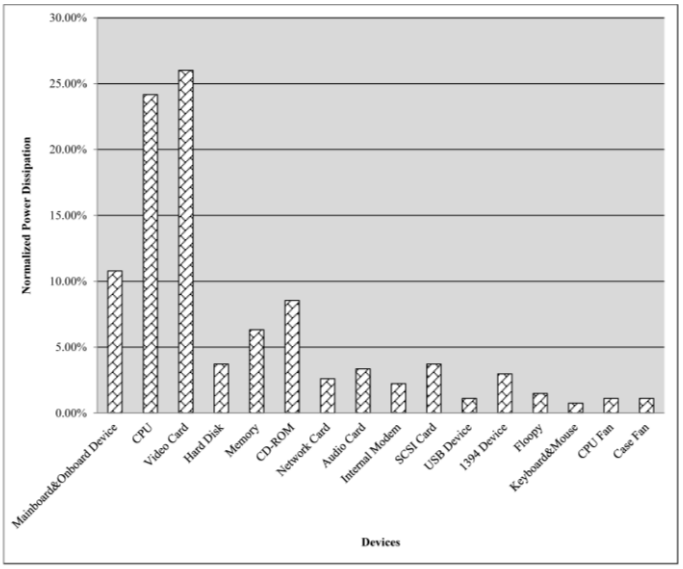

Fig 3. An example of computer power consumption

$$P_{total} = \sum_{i=0}^{n} \frac{U^2}{R} = \sum_{i=0}^{n} f \cdot U^2 \cdot C_{\text{dynamic\_capacitance}}, \quad (3)$$

where P_{total} is the total power consumption. n is the amount of the processors which are working, f is the clock frequency of one single processor, U is the voltage rating of the processor and $C_{\text{dynamic\_capacitance}}$ is the dynamic capacitance required to maintain Instructions per Clock Cycle (IPC) efficiency.

Since we should be working all the time, we can reduce CPU power consumption by turning several processors into sleep mode.

Thus, we get $P_{now} < P_{total}$, because $n < 4$.

3.2 Cost evaluation

The cost of a processor is proportional to the area of the chip. Due to the advancement of manufacturing chips, to same scale of transistors, new technology uses smaller area of chip compared to former technology. And it becomes more difficult to revolutionize the technology. However, our architecture only demand the former technology to produce CPUs, and easy to extend the scale of the system. Hence, cost of processors can be decreased.

In addition, the cost of optical fiber is getting lower and lower. So it won't be a costly organization to use optical printed circuit board.

3.3 Performance evaluation

The performance of our architecture depends on the frequency to switch the mode of processors. Each of the processor's performance equals its Frequency times Instruction per Clock Cycle [10].

$$Performance = Frequency \times Instructions\ per\ Clock\ Cycle \quad (4)$$

Thus, if the frequency to switch the mode of processors is not huge, the performance of the whole architecture can be relatively high.

4. Summary and conclusion

In this paper, the architecture for multiple processors on optical printed circuit board is presented. One of the processors controls other processors. With effective energy saving strategies including switching the mode of processors, assign tasks to different CPUs, using optical printed circuit board etc., we could reduce the power consumption and maintain a relatively high performance. However, some improvements such as limited processors amount etc. are needed for the proposed architecture.

Besides, the method is not limited to CPUs. It has a potential usage to GPUs and other similar chips which demand a great amount of power.

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