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## Realization of Flip Flops using LabVIEW and MATLAB

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### Abstract

Digital electronics is the backbone of current technology, play a pivotal role in the growth of humanity. Digital memory is part of digital electronics consists flip-flops building blocks designed by using logical NAND and NOR gates. Validation of storing information in form of bits can be understood from analysis of working of flip-flops. In the present investigation, VI Model of the different flip flops in LabVIEW has been realized and simulation implementation of flip flops is utilized to analyze the functioning of memory elements. The characteristics table of all kind of flip flop is verified using VI Models. Moreover, different flip-flops are also realized in MATLAB using Simulink. In the phase of digital and internet, this student -centric learning of existing theory of flip-flops can easily understand using simulation environment.

**Index Terms:** Flip-flop, Clock, LabVIEW, Boolean function, Simulation, Sequential circuits, Memory elements, Digital electronics, MATLAB, Simulink.

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### 1. Introduction

Simulation is not only just technology to test the functioning of a system for a set of inputs but also describe the behavior in the practical environment. It gives the view of designing, architecture, process before significant time and cost has been invested, and can be of the great benefit in support of technology implementation [1]. Simulation and modeling are getting knowledge about how a system will behave without actually testing in real life [2]. Simulation modeling provides a powerful methodology for advancing theory and research on complex behaviors and systems [3]. Simulation provides a way to actively engage scholar in making and testing conjunctures about data, developing their reasoning about electronic concepts and procedures. Simulation can encourage them to develop their analytical reasoning by requiring them to analyze

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processes and set up a series of outcomes (i.e. modeling) [4]. In order to reduce costs, improving quality, and shortening the time-to-market for manufactured goods, simulation plays a vital role. The development of new simulation interface standards could help increase the development of simulation technology [5]. Digital electronics is used fundamental scientific computation and internet of things. To provide the platform to students, to test their ideas through simulation laboratory using Labview/Matlab, this paper presents simulation design of different flip flops i.e R-S, J-K, D, T flip-flops using LabVIEW-VI Models [6],[7],[8].

### 1.1. LabVIEW Simulation Tool

LabView stands for Laboratory Virtual Instrument Engineering Workbench. In LabView, the Models developed for a solution of given mathematical or logical problem using graphical programming are known as VI's and every VI uses various functions that manipulate and map input from the user end and display that information, move it to other files or other computers. To do work with LabView, first, open LabView version and create a project for your work. Every VI block contains the three components:

- *Front Panel*

In Fig.1, shows an example of front panel [6]. Front panel have numeric, Boolean, string and path array matrix, list table and graph, ring and enum containers I/O variant and CI decoration enum etc

- *Block Panel*

It contains graphical source code to describe the functionality of the VI. Front panel objects appear as terminals on the block diagram. Block diagram comprises structures, array, cluster, numeric, Boolean, string comparison, timing, dialog & use, file I/O, waveform application, synchronization, graphics etc.

- *Icon & Connector Panel*

It can be used to identify the VI so that another VI (sub-VI) can be used in VI. Sub VI role is similar to the subroutine in the text - based G programming languages [6]. LabView have a great scope in various areas, to bridging the gap between theories and their practical implementation. LabVIEW is mainly used in data acquisition interface with hardware. The domain and type of usage of virtual platform LabVIEW is depicted in Fig. 1.

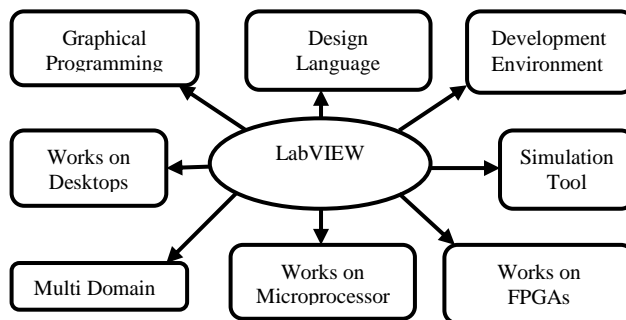


Fig.1. Usage of LabVIEW

In the previous section, an overview of LabVIEW has been described. In forthcoming section 2 and in section 3, digital circuits systems are classified and flip-flops with their designs using logical gates have been

presented.

## 2. Types of Digital Circuit Systems

Digital electronics are backbones in electronics and electrical technology in current epoch [8], [9], [10], [11], [12], [13]. In Fig.2, the classification of Digital circuits is depicted and described below.

*Combinational Digital Circuits:* Only present states of input determine the outcome of combinational devices.

*Sequential Digital Circuits:* Sequential digital circuit includes combinational digital circuit in forward path and memory elements in feedback path. Fig.3 shows the block diagram of sequential digital circuit.

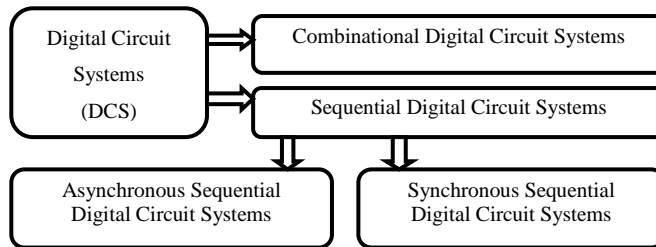


Fig.2. Classification of Electronic Digital Circuits

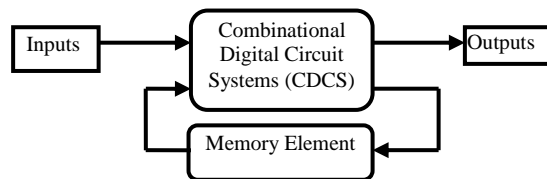


Fig.3. Block Diagram of Sequential Circuit

### 2.1 Memory Element (ME)

The memory elements are the flip-flops or latches to store binary information in form of bits. State of the flip-flops define either stored or to store binary information. A state may present state (PS) or next state (NS), which stored in the memory element. Digital circuit systems have the memory elements are known as sequential logic circuits.

### 2.2 Sequential Logic circuit

Outputs of the sequential digital circuit depend upon external inputs and output of the memory elements. Sequential logic circuits are two types' synchronous sequential logic circuit and asynchronous sequential logic circuit. Synchronous Sequential logic circuits are those digital circuits whose behavior can be defined from the knowledge of its signals (inputs and present state) at synchronous time intervals.

## 3. Design and Analysis of Latch

### 3.1. Latch using NOR gate

Digital devices may need memory element to carry the previous state of the output. Memory elements can store binary information [1], [2], [3], [9], [10]. Flip-flop is used as the memory element. A latch is an asynchronous circuit where two inputs(S-set and R-reset) and two outputs Q and Q', both are a complement to each other. The feedback path is made by cross-coupled connection from the output of the second gate back to the input of the first gate and vice versa.

Working on latch: It may be design either using NOR or NAND gates. The working of latch is described as below:

- Step 1: If SR inputs are 1 and 0 then output Q is 1: NOR Gate-1, consist of two inputs first come from reset is 0 and other from the output of NOR gate-2 is 0 and the output Q is 1. Similarly, NOR gate-2, consist of two inputs comes from the set is 1 and other from the output of NOR gate-1 is 0 and the output Q' is 0.
- Step 2: If SR inputs are 0 and 1 then output Q is 0: NOR gate G1, consist of two inputs first comes from reset is 1 and other from the output of NOR gate-2 is 0 and the output Q is zero. Similarly, NOR gate-2, consist of two input comes from set is 0 and other from output of NOR gate-1 is 0 and the output Q' is 1.
- Step 3: If SR inputs are 0 and 0 then the output Q is 0: NOR gate G1, consist of two inputs, first come from reset is 0 and other from the output of NOR gate-2 is 1, then the output Q is 0. Similarly, NOR gate-2, consist of two inputs comes from the set input is zero and other from output of NOR gate-1 is 0 and the output Q' is 1.
- Step 4: If SR inputs are 1 and 1 then output Q is not determined: NOR gate G1, consist of two inputs first come from reset is 1 and other from the output of NOR gate-2 are 1; Similarly, NOR gate-2, consist of two inputs comes from set is 1 and other input from the output of NOR gate-1 is 0; As for both NOR gates, one input is already 1, so no one will wait further and both try to give output Q and Q' as 0. That's why it is almost impossible to predict the output. S-R latch comprising of NOR gates has been shown in Fig.4.

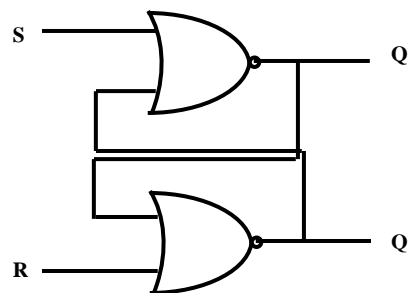


Fig.4. Design of Latch Using NOR Gates

The working of latch comprise the nor gates, can be summerised in Table 1.

Table 1. Characteristic Table of RS Flip-Flop

S	R	Q	Q'
1	0	1	0
0	1	0	1
0	0	0	1
1	1	-	-

### 3.2. Realisation of Latch using NAND Gate

The design of latch using NAND gates is depicted in Fig.5.

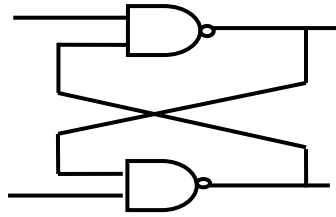


Fig.5. Fundamental Flip-Flop with NAND Gates

Basic latch have two NAND gates in which S, R are inputs and Q, Q' as outputs. The G1 have two inputs, one is input S and another from the output Q' of G2. G2 gate also have two inputs, one is R and another from output Q of G1. Initially, Reset input kept logical 1 and Set at logical 0. Due to these inputs, the normal output returns to logical 1 and Q' goes to logical 0. Now if both input Set and Reset has shifted to logical 0, the normal output remain logical 1 and Q' remain logical 0. Hence at S=0 and R=0, the latch behave like the memory element. If the Reset is at logical 1 and Set is at logical 0 then the normal output becomes logical 0 and inverted output becomes logical 1, are known as the clear state of the memory element. By shifting the S input to logical 0 and R input to logical 0, the outputs remain same present state.

It is strongly recommended that the both input S and R never fed logical 1, since both output returns to logical 0, which is inconsistency with normal and inverted output of the latch the behavior of variation of output with changes in inputs of the latch is depicted in Table 2.

Table 2. Characteristic Table of SR Flip-Flop

S	R	Q	Q'
1	0	0	1
1	1	0	1
0	1	1	0
1	1	1	0
0	0	1	1

### 3.3. Clocked RS Flip-Flop

The latch or basic flip flop discussed above is an asynchronous sequential circuit and if a clock is used in such latches, then it is known as a synchronous sequential circuit, depicted in Fig.6 as clocked R-S flip flop. It has two AND neither gates, two NOR gates. G1 AND gate have two input, one is R and second clock pulse, and G2 the AND gate also consist two input R and CP, the output of G1 fed to G3 NOR gate and output of G2 to G3 NOR gate. Logical AND gate gives output 0 if either of input is 0, output 1 if all inputs are logical 1. If clock Pulse is zero, the output of the G1 and G2 AND gates remain logical 0 because the output of the G1 and G2 are connected to G3 and G4, regardless of S and R input values. When clock is one, information from S and R inputs allowed to reach to the SR latch, if S is 1 and R are 0, CP=1, flip-flop returns to set, and normal output becomes logical 1, inverted output logical 0, are known as set the state of clocked RS flip-flop. The truth table of SR flip-flop is represented in Table3.

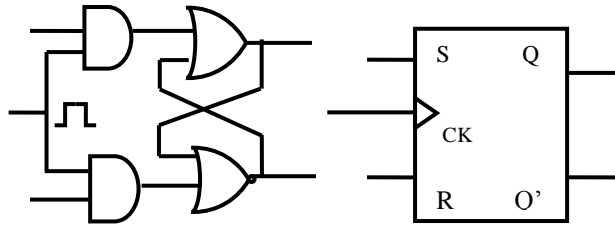


Fig.6. Circuit for SR Flip-Flop (Clocked) and Symbol of clocked SR Flip-Flop

Table 3. Characteristic Table of SR Clocked Flip-Flop

$Q_n$	S	R	$Q_{n+1}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	Indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Indeterminate

### 3.4. D Flip-Flop

D flip-flop is modified version of SR flip-flop, and it is depicted in Fig.7, consists input D and inverted D using G5 NAND gate.

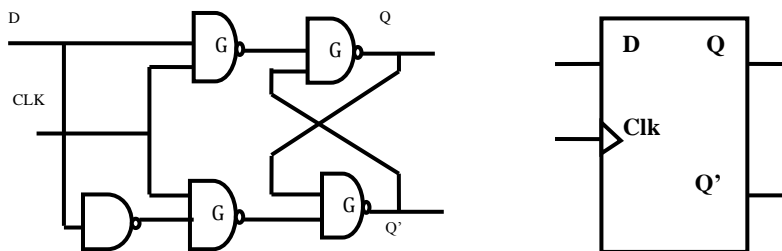


Fig.7.Logic Diagram D Flip-Flop using NAND Gates and Graphical Representation of D Flip-Flop

## 4. Implementation Of RS Latch Using LabVIEW and MATALB

In this section, different flip-flops are developed using Labview VI models[11], [14].

### 4.1. Asynchronous RS Flip-Flop Using NOR Gate

In Fig.8, VI model of RS flip-flop has RS as inputs and Q and Q' as outputs, with cross-feedback connections is developed in block panel LabVIEW.

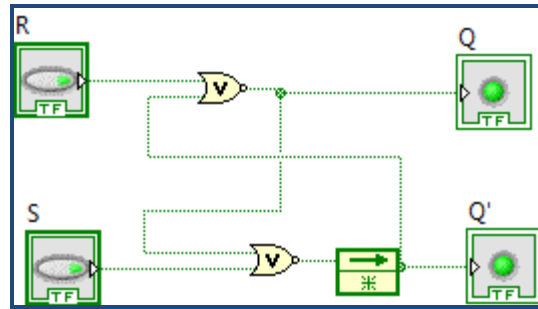


Fig.8. Fundamental Memory Element with NOR Gates VI Model Using Labview

Design of R-S Latch Using MATLAB-Simulink: In Fig.9, the Simulink model of R-S latch is depicted.

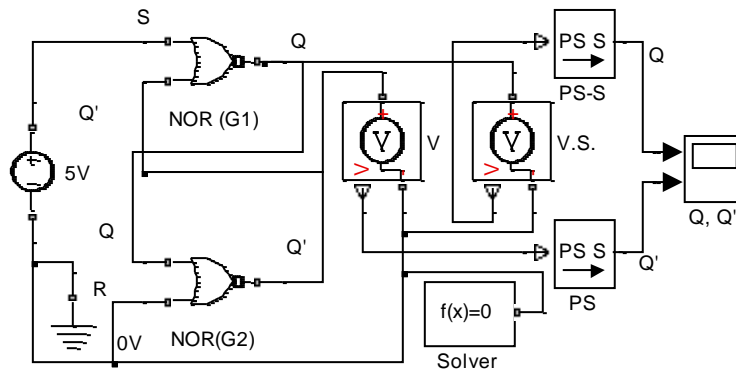


Fig.9. R-S Latch Realization Using NOR gates in MATLAB-Simulink Environment

#### 4.2. RS Latch Using NAND Gates in VI Model

LabVIEW VI model of RS flip-flop using NAND gate is shown in Fig.10 which consist two NAND gate, with cross-feedback and S and R inputs.

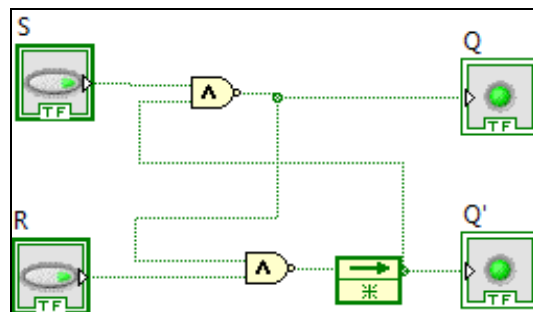


Fig.10. SR Flip-Flop Using NAND Gate in VI Model

4.3. Design of S-R Latch Using Simulink in MATLAB

The Matlab Simulink’s model of S-R latch flip-flop is depicted in Fig.11. The model is developed in a graphical user-friendly environment known as Simulink.

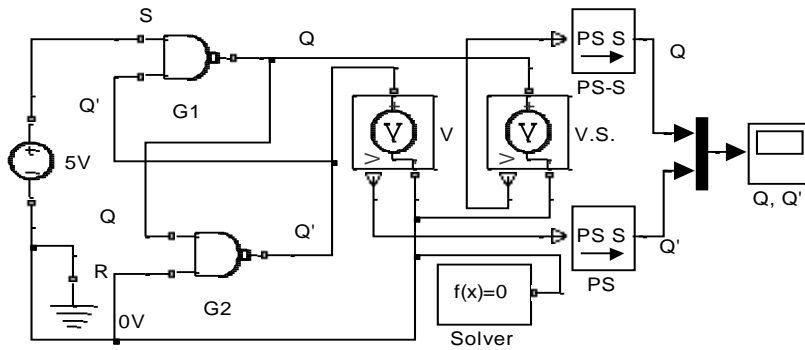


Fig.11. MATLAB-Simulink Model of S-R Latch

4.4. Clocked R-S Flip Flop VI Model

In Fig.12, LabVIEW VI model for clocked RS Flip-Flop is depicted. This shows the analysis report for the clocked RS VI model, where light green colour shows the logic 1 and blackish colour shows the logic 0.

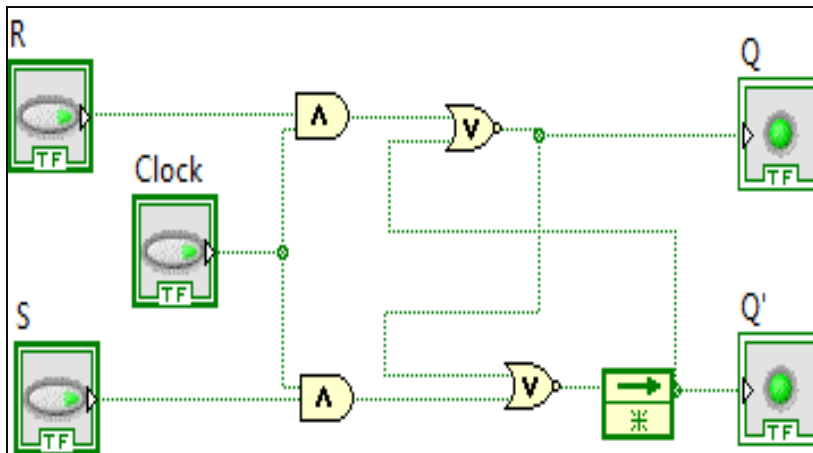


Fig.12. VI Model of Clocked RS Flip-Flop

4.5. VI Model of RS Flip-Flop Consists NAND Gates

The VI model of RS flip-flop using universal NAND gate has designed and depicted in Fig.13.



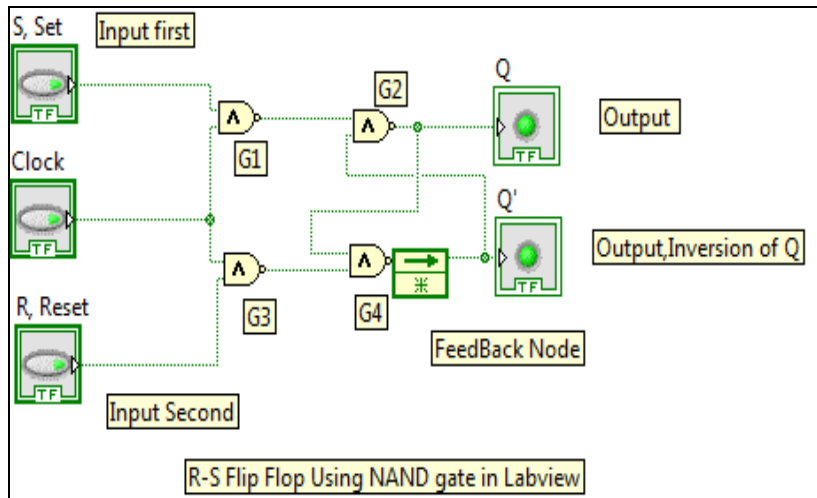


Fig.13. VI Model of RS Flip-Flop Using NAND Gate

#### 4.6. VI model of JK Flip-Flop

The VI LabVIEW model of JK flip-flop VI is depicted in Fig.14, consists J, K as inputs and clock as the control variable, Q and Q' two outputs. An output of J-K flip-flop is a function of inputs and present state of the flip-flop.

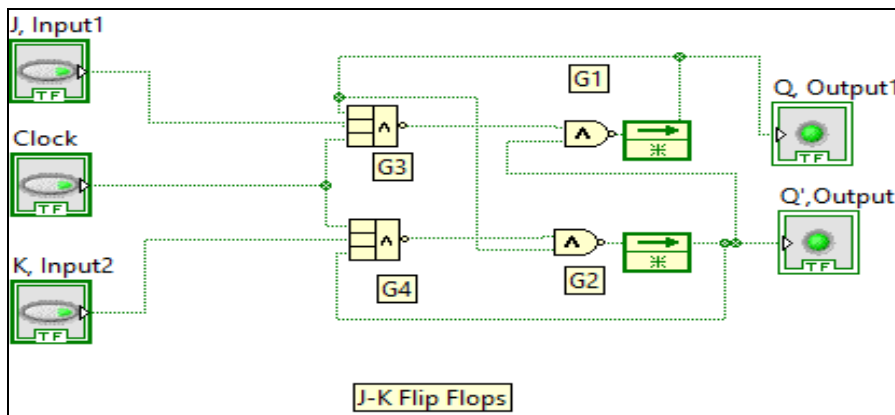


Fig.14. VI Model of JK Flip-Flop Using NAND Gates

#### 4.7. VI Model of D Flip Flops

D stands for a delay in the input signal, and the D flip-flop as VI model in LabVIEW using AND, NOR, NAND gates has been depicted in Fig.15.

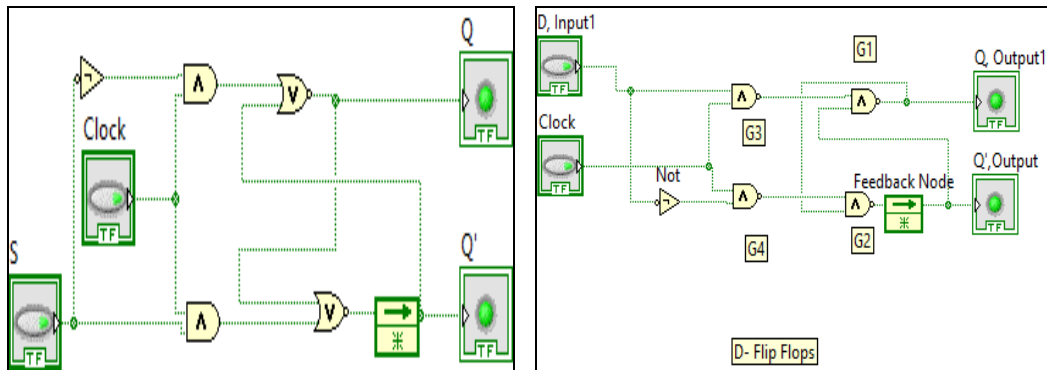


Fig.15. VI Model D Flip-Flop Using AND, NOR Gates and another model using NAND gates

4.8. VI Model T Flip-Flop

T stands for toggle and T flip-flop is modified version of JK flip-flop, depicted in Fig.16.

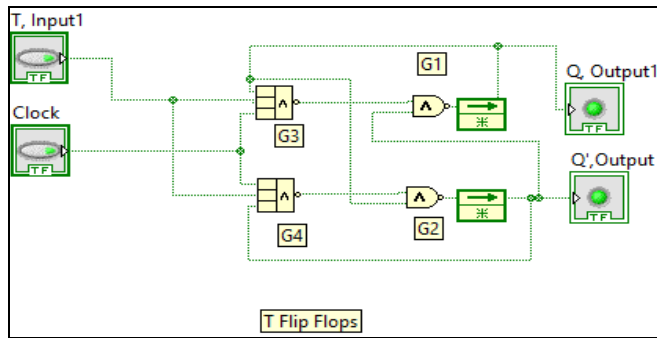


Fig.16. VI Model of T Flip-Flop

4.9. J-K Flip Flop Using MATLAB-Simulink

The Simulation model of the J-K flip-flop in MATLAB-Simulink is designed and depicted in Fig.17.

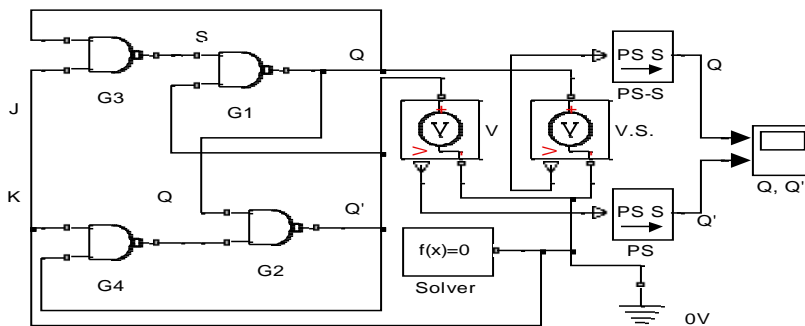


Fig.17. MATLAB Simulink Model of J-K Flip Flop

4.10. VI Model of Master Slave JK Flip-Flop

VI model of master-slave JK flip-flop using LabVIEW has been depicted in Fig.18.

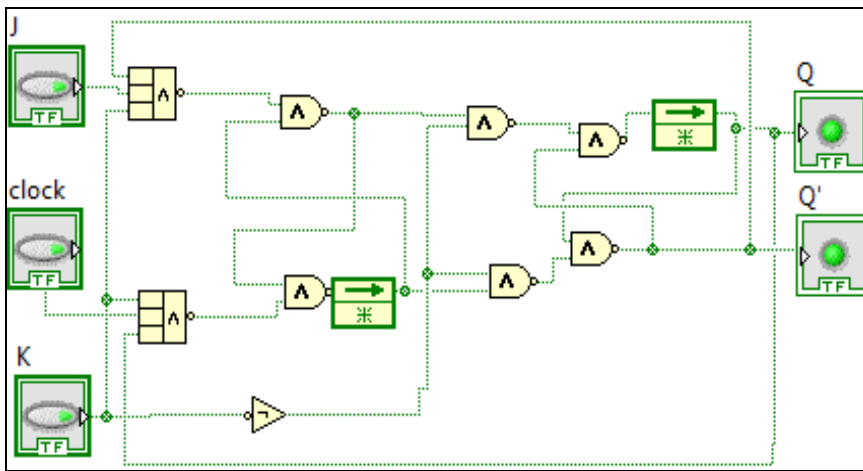


Fig.18. VI Model of Master Slave JK Flip-Flop

5. Results And Conclusion

In Fig.19, Output simulation result of VI.Model of SR latch composite of NOR gated depicted in Fig.8. From the VI.Model of NOR-based 1 S-R latch, it is observed, input S-R tempted the output Q and Q'.

- First Observation: If S is kept high and R low, the output Q is high and Q' is low
- Second Observation: If S and R both kept low, out remain the same pervious state.
- Third Observation: If S keep low and R at high, result output Q goes to low and Q' become high.
- Fourth observation: If both input S and R are high then both of output low as shown in Fig.21, clearly it is undefined state of S-R latch.

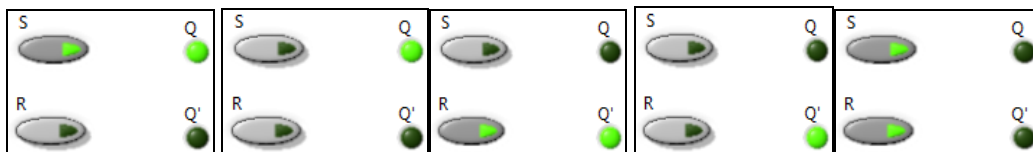


Fig.19. Simulation Output of SR flips-flop using VI.Model

In Fig.22, output simulation result of VI.Model of SR latch composite of NAND gates depicted in Fig.9. The Logical input to R and S is 0 or 1, predict Q and Q'. It is observed in Fig. 21, R kept high, and S low, the output Q is high and Q' is low. Secondly, when both of inputs S-R are high, output remains as previous state. Thirdly, if R is low and S high, then output Q high and Q' low as per observation from Fig. 19, Moreover, if both of R-S kept low, turns both output high, which is a case of the undetermined.

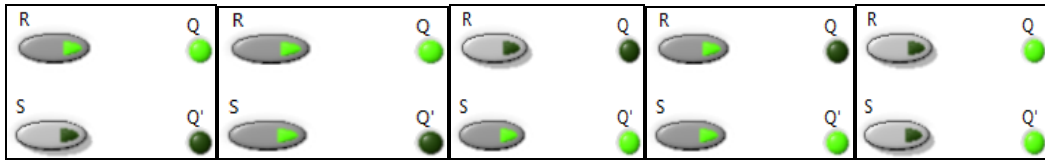


Fig.20. Clocked RS Flip Flop Fed with Low Clock and High Clock, Simulation Output of the Low Clock

In Fig.21, simulation output result of VI.Model of R-S flip-flops is depicted. Firstly, the flip-flop is analyzed for a clock of the state. It is observed that if clock is low, output does not change with the change in inputs R-S as clear from Fig. 21(a). The generic R-S flip-flop operation took place when the clock kept high as shown in Fig.21 (b). The working of the R-S flip flop as according to change in R-S inputs, output is obviously observed in Fig. 21(b). First observation, R kept high and S low, the output Q is low and Q' high, Second observation, if both input kept low then output remain same as according to previous state. Thirdly, if R is low and S high, then the output Q turns high and Q' become low as per observation. Fourthly, if both input change to high, then the output Q and Q' become low which is an undefined condition of S-R flip-flops.

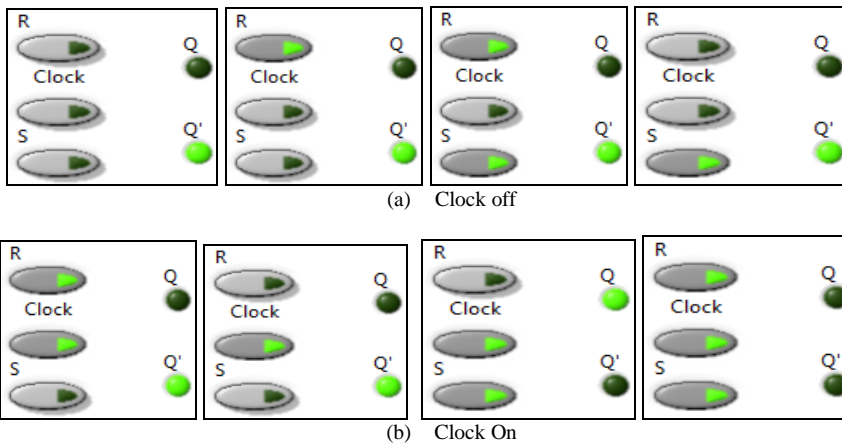


Fig.21. Front Panel logical analysis of Clocked RS Flip-Flop using NOR Gates

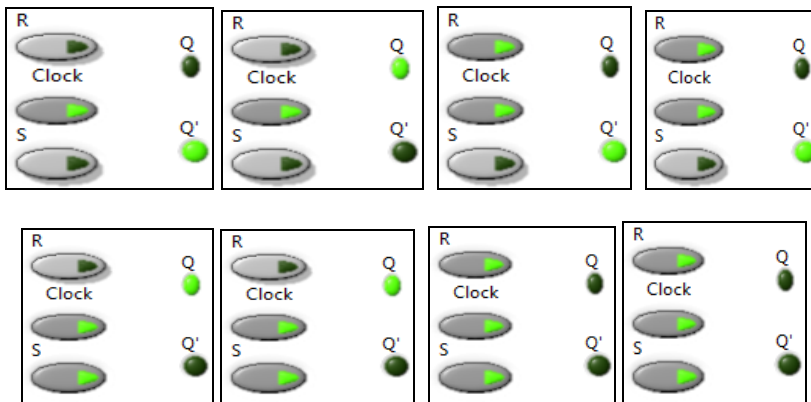


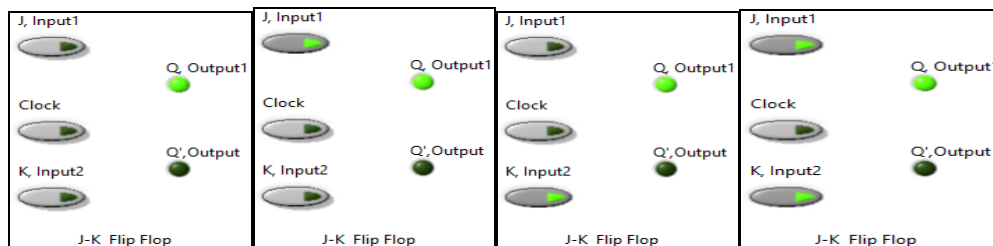
Fig.22. Front Panel VI Model of RS Flip-Flop Clocked using NAND gates

Simulation output result of R-S flip flop is concluded in Table 4.

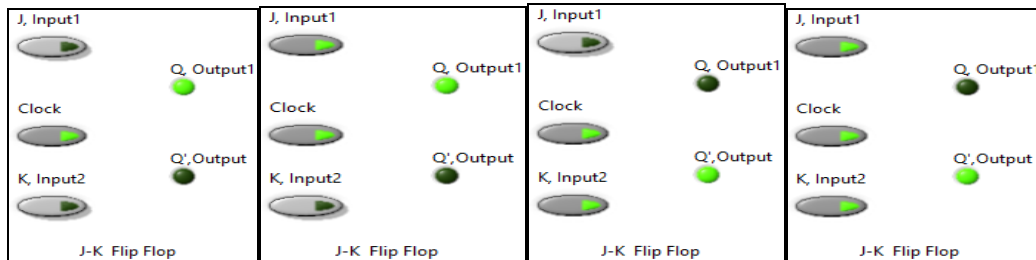
Table 4. RS Flip-Flop Truth Table verified using Labview

S. No.	RS Flip-Flop				
	Clock	S, Input	R, Input	Q, Output	Q', Output
1	0	0	0	1	0
2	0	1	0	1	0
3	0	0	1	1	0
4	0	1	1	1	0
5	1	0	0	1	0
6	1	0	1	0	1
7	1	1	0	1	0
8	1	1	1	1	1

The simulation output of J-K flip-flop of VI.Model on the execution of Fig.14 is depicted in Fig.23.



(a) VI Model (Front Panel) JK Flip-Flop (Clock off)



(b) VI Model (Front Panel) JK Flip-Flop (Clock on)

Fig.23. Simulation Results J-K Flip-flop VI.Model

Observations of Fig.25 are depicted in Table 5.

Table 5. JK Flip-Flop Truth Table verified using Labview

S. No.	JK Fli-Flop				
	Clock	S, Input	R, Input	Q, Output	Q', Output
1	0(off)	0	0	1	0
2	0(off)	1	0	1	0
3	0(off)	0	1	1	0
4	0(off)	1	1	1	0
5	1(on)	0	0	1	Q <sub>n</sub>
6	1(on)	0	1	0	1
7	1(on)	1	0	1	0
8	1(on)	1	1	1	Q <sub>n</sub> '

The characteristics behavior of D flip-flop is depicted in Fig.24. It is versatile memory element used in counter designs.

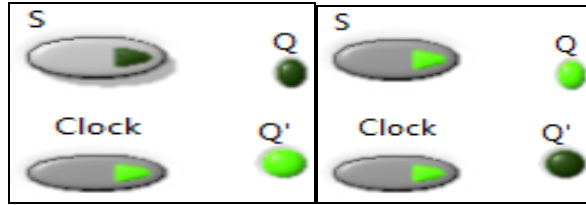


Fig.24. VI Model (Front Panel) of D Flip-Flop

In Fig. 25, the output simulation result of S-R Latch composite of NAND gates designed in MATLAB-Simulink, Fig.11 is depicted.

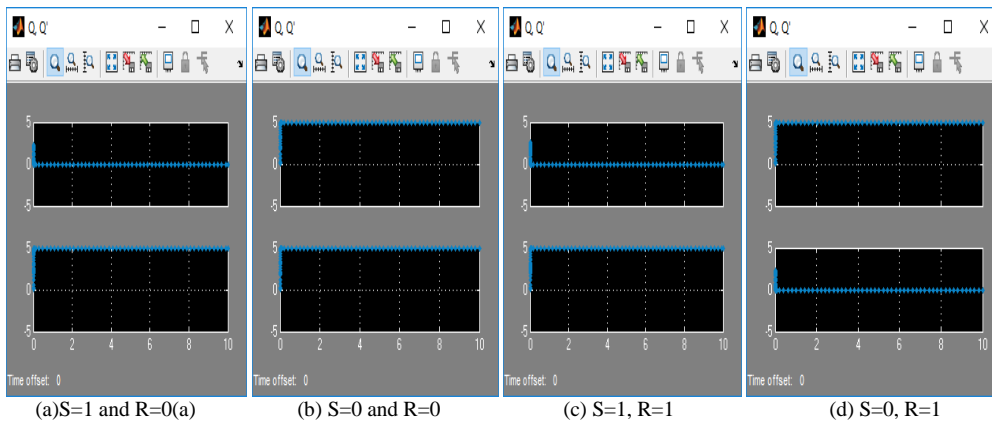


Fig.25. S-R Latch Simulink Simulation Output

In Fig.26, Simulation output result J-K flip modelled in MATLAB Simulink is depicted. It is noticed that in first observation by keeping J=0 and K=0, the output are high for Q' and low Q. Now different combination of input-output is determined their representation clearly depicted in Fig.29.

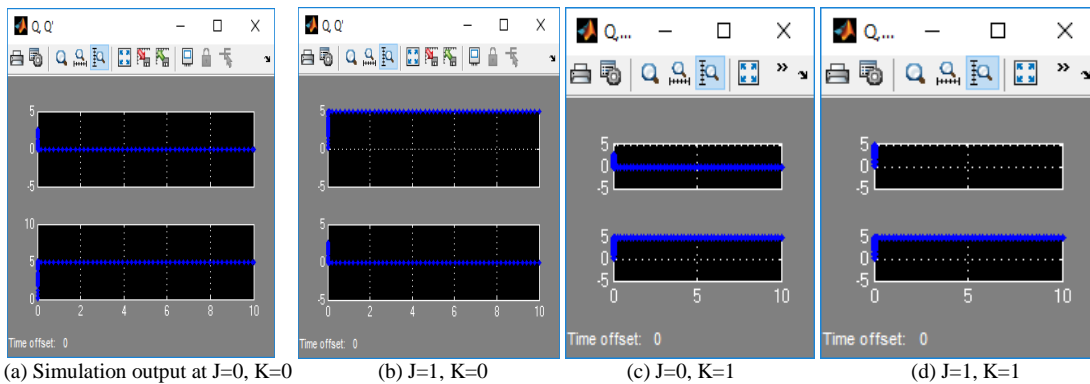


Fig.26. Output Result MATLAB Simulink Model of J-K Flip-flop

Operations of flip-flop circuits are verified using the LabVIEW and MATLAB. Different flip-flops are explained with their characteristic table in theoretically and virtually in VI models and MATLAB Simulink models. A student centered learning is developed, to create the interest of the student in the modeling of digital circuits and systems and in horizontal and vertical curricula for the different domain of subjects at the graduate level and postgraduate level. It is also observed that it is easy to study flip-flops in LabVIEW than MATLAB.

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**Sunita Rani** was born in Haryana on October 14, 1989. She received her B.Tech. Degree in Electronics & Communication Engineering from Ch. Devi Lal University, Sirsa, Haryana in the year 2011. She received her Master in technology (M.Tech.) in VLSI Design from YMCA University of Science & Technology, Faridabad, Haryana in 2014. Presently she is working in the Department of Electronics and Communication Engineering in Bhagat Phool Singh Mahila Vishwavidyalaya, Khanpur Kalan, Sonapat, Haryana, India. Her area of interest is design VLSI chip and she also works for Quantum Dot Cellular Automata technology for VLSI design.

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