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Design of Low Power Test Pattern Generator using Low Transition LFSR for high Fault Coverage Analysis

Chethan J, Manjunath Lakkannavar
VTU Extension Center, UTL Technologies Ltd, Visvesvaraya Technological University, Bengaluru, Karnataka, India
chethan163@gmail.com, manjulakkannavar@gmail.com

Abstract —A low power Test Pattern Generator (TPG) designed by modifying Linear Feedback Shift Register is proposed to produce low power test vectors that are deployed on Circuit under Test (CUT) to slenderize the dynamic power consumption by CUT. The technique involved in generating low power test patterns is performed by increasing the correlativity between the successive vectors; the ambiguity in increasing the similarity between consecutive vectors is resolved by reducing the number of bit flips between successive test patterns. Upon deploying the low power test patterns at the inputs of CUT, slenderizes the switching activities inside CUT that in turn reduces its dynamic power consumption. The resulted low power test vectors are deployed on CUT to obtain fault coverage. The experimental results demonstrate significant power reduction by low power TPG than compared to standard LFSR.

Index Terms—ATPG, CUT, EDA, FAULT COVERAGE, LFSR, TPG, TEST VECTOR, VERILOG.

I. INTRODUCTION

With the immense ongoing technological developments in Very Large Scale Integration (VLSI) domain has led Application Specific Integrated Circuit (ASIC) design technology to increase density of gates per Integrated circuit(IC) and the processing speed of the Integrated circuit with limited area and low power consumption. As the design density increases the need for testability of Integrated circuit design has become mandatory. Designing and testing of very large Integrated circuit designs can be carried out with the Electronic Design Automation (EDA) software tools. The testing of Integrated Circuits with random test patterns will result in high power dissipation in test mode which is hazardous to functionality of integrated chip [1]. The promising solution to reduce power dissipation is low power testing methodology.

Various authors have carried their research in optimizing Test Pattern Generator design to reduce the power consumption by Circuit under Test while testing for stuck at faults. A Low Transition Galios Linear Feedback Shift Register (LT - GLFSR) composed of modified GLFSR to reduce transitions in Circuit under Test (CUT) as compared to standard Linear Feedback Shift Register (LFSR) and Galios Linear Feedback Shift Register (GLFSR) presented in [1],[4].

Reference [3] reveals a low power test pattern generator design combines a gray counter and Read Only Memory (ROM) to produce low power patterns acting on CUT, resulting 52% reduction of dynamic power consumption.

Reference [2], presents a new low power LFSR for Built in Self Test (BIST) that utilizes bit swapping technique to reduce transitions inside CUT, exhibiting 27.48% reduction in dynamic power consumption than compared to standard LFSR. The design was simulated using Cadence Electronic Design Automation (EDA) tool in 180nm technology.

The Low Transition Random Test Pattern Generator (LT-RTPG) reduces switching activity of CUT by reducing transitions during scan testing is presented in [5], [6], [7]. Various other low power TPG architectures are proposed for scan inserted Built In Self Test (BIST) are presented in [8], [9], [10] and for full scan operation mode in [11], [12].

The low power test pattern generator presented in [13] depicts cellular automata TPG architecture that reduces the test power in combinational circuits. The low-power test pattern generator based on a modified LFSR is proposed in [14], [16]. This modified LFSR architecture adds weights to the vectors, decreases power consumption and increases fault coverage. A low power BIST for data path architecture, built by utilizing multiplier and accumulator pairs, is proposed in [15].

The presented work proposes a low power Test Pattern Generator (TPG) to reduce the dynamic power consumed by Circuit under Test (CUT). The proposed design is designed and simulated using industry standard Cadence simulator and Cadence RTL compiler to validate its correct functionality and Automatic Test Pattern Generator (ATPG) EDA tool is used to attain 100% Fault Coverage of CUT in 90nm technology. The design technique increases the correlation between successive test patterns to slenderize switching activity in Circuit under Test (CUT) which in turn decreases overall dynamic power consumption of CUT during test mode.

The next section briefly describes the overall flow of the steps involved or the work presented in this paper. Further the third section reveals the key idea/technique

behind generating low-power test vectors. This technique is modeled into a logical architecture in fourth section, and it also reveals the concept of generating control signals involved in generating low power vectors. The low power architecture is then implemented using ASIC (Application Specific Integrated Circuit) design approach and the implementation, RTL Schematic, simulation and power consumption results are depicted in fifth section. Finally the overall work flow is concluded in the last section.

II. METHODOLOGY

The low power pattern generation technique is embedded onto an LFSR to create the proposed low power Test Pattern Generator (TPG). The design and power consumption report of the Conventional LFSR and proposed low power Test Patterns Generator (LP-TPG) is obtained using industry standard Cadence RTL compiler tool.

The proposed low power Test Pattern Generator (TPG) design increases the correlation between test patterns to reduce the primary inputs (PIs) switching activities which eventually scale down the transitions inside the Circuit under Test (CUT), and hence power consumption.

Thereafter the test pattern generated by both Conventional LFSR as well as low power Test Patterns Generator (TPG) designs are made to run on Circuit under Test (CUT) individually. C432 International symposium on Circuits and Systems (ISCAS 84) benchmark circuit is chosen as Circuit under Test (CUT) in order to obtain its power consumption during test mode. Further fault simulation is performed on Circuit under Test (CUT) upon deploying low power test patterns at its Primary Inputs (PIs); this process is again iterated on CUT with standard LFSR pattern to obtain desired fault coverage.

III. LOW POWER PATTERN GENERATION TECHNIQUE

The intent behind generating low power pattern is to reduce total number of bit flips between successive test patterns which avoids maximum transitions at the inputs of Circuit under Test (CUT) leading to slenderize switching activity inside CUT. The technique implies LFSR with an additional circuitry is utilized to accomplish the generation of low power test vectors by inserting intermediate patterns between successive test vectors.

Let's assume that $\mathbf{P^i} = \{ b^i_1, b^i_2, b^i_3, \ldots, b^i_i, \ldots b^i_n \}$ and $\mathbf{P^{i+1}} = \{ b^{i+1}_1, b^{i+1}_2, b^{i+1}_3, \ldots, b^i_i, \ldots b^{i+1}_n \}$ are the consecutive test vectors, where $\mathbf{P^{i+1}}$ is derived by simply right shifting all bits $\mathbf{P^i}$.

$\mathbf{P^{i1}} = \{ b^{i1}_1, b^{i1}_2, b^{i1}_3, \ldots\ldots\ldots, b^i_i, \ldots\ldots\ldots b^{i1}_n \}$,

$\mathbf{P^{i2}} = \{ b^{i2}_1, b^{i2}_2, b^{i2}_3, \ldots\ldots\ldots, b^i_i, \ldots\ldots\ldots b^{i2}_n \}$

and

$\mathbf{P^{i3}} = \{ b^{i3}_1, b^{i3}_2, b^{i3}_3, \ldots, b^i_i, \ldots b^{i3}_n \}$ are intermediate test vectors inserted between $\mathbf{P^i}$ and $\mathbf{P^{i+1}}$. These intermediate vectors are generated by splitting the vector set into two equal halves which are depicted in below fig. 1.

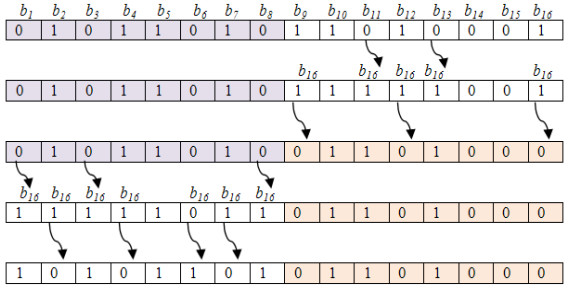

Figure 1: Low power pattern generation technique.

This process starts with the generation of vector P^{i2} in between P^i and P^{i+1} and it is generated by placing first half of P^i at first part of P^{i2} and second half of P^{i+1} at the second part P^{i2}.

$$\mathbf{P^{i2}} = \{ b^{i2}_1, b^{i2}_2, \ldots\ldots b^{i2}_{(n/2)}, b^{i2}_{(n/2)+1}, \ldots\ldots b^{i2}_n \}$$
$$= \{ \underbrace{b^i_1, b^i_2, \ldots b^i_{(n/2)}}_{\text{First half of } \mathbf{P^i}}, \underbrace{b^{i+1}_1, b^{i+1}_2, \ldots b^{i+1}_n}_{\text{Second half of } \mathbf{P^{i+1}}} \} \quad (1)$$

The test vector P^{i1} is generated between P^i and P^{i2}. It is produced by positioning first half of P^i at first part of P^{i1} and second part is developed by comparing second half part P^i with P^{i2}, if bits are similar then same bits will be retained otherwise last bit of P^i (b^i_n) is positioned.

$$b^{i1}_{(n/2)+j} = \begin{cases} b^i_j & \text{if } (b^i_j = b^{i2}_j) \\ b^i_n & \text{if } (b^i_j \neq b^{i2}_j) \end{cases} \quad (2)$$

Similarly P^{i3} is produced between P^{i2} and P^{i+1}, first half is placed by comparing first half of P^{i2} with first half of P^{i+1} and the second half is positioned by second half of P^{i+1}. The above fig. 1 depicts a 16 bit low power test patterns that have not more than four transitions between successive test vectors.

IV. DESIGN OF LOW POWER TEST PATTERN GENERATOR

The low power pattern generation algorithm depicted in section 3 is coded using Hardware Descriptive Language (HDL) labeled Verilog with initial seed vector loaded as pre-initial stage to the TPG. Fig. 2 depicts 8-bit low power Test - Pattern Generator (TPG) composed of extrinsic XOR based Linear Feedback Shift Register (LFSR) along with an appended combinational logic to produce low power test vectors. Combinational logic consists of logic blocks and multiplexers (MUX) connected to the output of D – Flip flops in LFSR. The internal architecture of logic block

is very simple as shown in fig. 3, it consists of an AND gate and an OR gate with their output connected to the inputs of MUX.

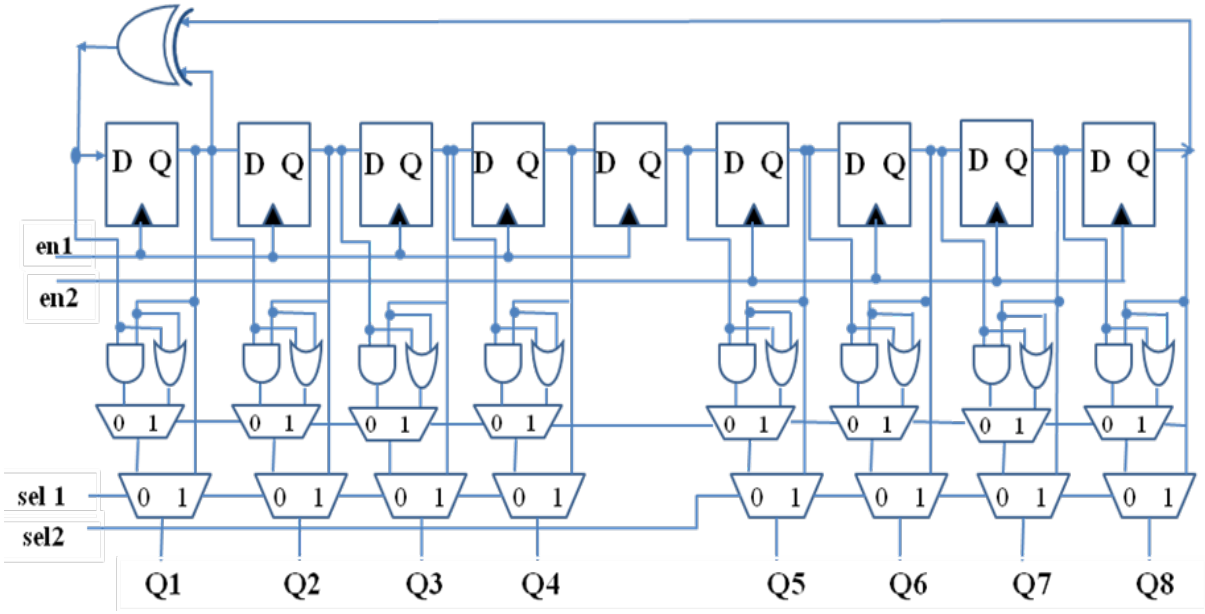

Figure 2: Low power Test Pattern Generator (TPG).

4.1 Design of Finite State Machine

The state machine depicted in fig 4 incorporates four states to produce control signals to drive TPG to generate low power vectors are explained as follows:

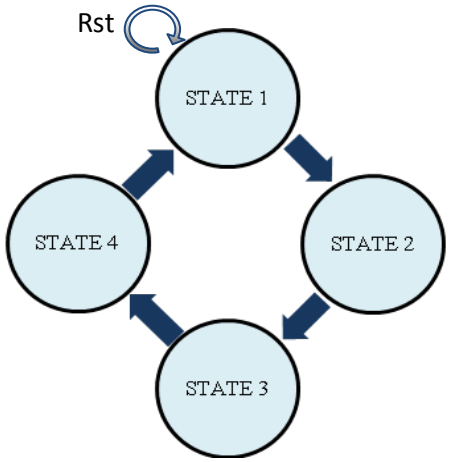

Figure 3: Finite State Machine (FSM).

Table 1: Control signals generated by FSM

STATE	en1	en2	sel1	sel2
1	1	0	1	1
2	0	0	1	0
3	0	1	1	1
4	0	0	0	1

Table 1 represents the control signals generated by the above designed Finite State Machine (FSM).

State 1: In first state the FSM outputs control signals (en1 = 1, en2 = 0, sel1 = 1, sel2 = 1). The en1 enables the shift operation at the first half of LFSR whereas en2 signal disables second half of LFSR. The sel1 and sel2 in active high state tends MUX to fetch the output of D Flip Flops in Linear Feedback Shift Register (LFSR). Thus generating first test vector P^i at output of TPG.

State 2: At the second stage FSM produces (en1 = 0, en2 = 0, sel1 = 1, sel2 = 0). With en1 and en2 in active low state, the LFSR remains idle by outputting previous stored values. The sel1 signal outputs first half of P^i and sel2 signal tends MUX to compare the present bit value with the previous bit value; if the bits are similar, present bit value is outputted otherwise last bit of P^i is omitted to the output of TPG (P^{i1} vector is produced).

State 3: The third FSM state generates (en1 = 0, en2 = 1, sel1 = 1, sel2 = 1). First half of LFSR remains idle with previous data at its output and the second half of it performs shift operation. Then the control signals sel1 and sel2 in active high state tends MUX to select the output of D-Flops. Thus generating third test vector P^{i2} at output of TPG.

State 4: The final state produces (en1 = 0, en2 = 0, sel1 = 0, sel2 = 1). With active low en1 and en2 signal no shift operation is performed by LFSR thereby it remains in previous state. The active low sel1 signal tends MUX to compare the present bit value with the previous bit value; if bits are similar present bit value is outputted otherwise last bit of P^i is omitted to the first half output of TPG and second half is positioned by output of D-Flops. Hence this state produces test vector

P^{i3}. The above process continues cyclically by going through STATE 1 to produce P^{i+1}.

V. IMPLEMENTATION

The low power test pattern generator (TPG) depicted in fig. 2 is designed in Verilog language using industry standard Cadence RTL compiler with 90nm Deep Sub Micron (DSM) technology library. The design is synthesized upon applying suitable timing constraints to generate Register to transistor level (RTL) netlist as depicted in fig. 4.

Similarly standard Linear Feedback Shift Register (LFSR) netlist is generated using the aforementioned timing constraints. Fig. 4 and fig.5 depicts the netlist generated for low power Test Pattern Generator (TPG) and standard Linear Feedback Shift Register (LFSR) respectively.

Further the low power patterns are fed as an input to the primary inputs of the CUT (Circuit Under Test), the switching activities inside the CUT is dumped in to an EVCD (Extended Value Change Dump) file which is read as the test vectors by ATPG (Automatic Test Pattern Generator) Tool in order to obtain fault coverage for CUT. Similarly the EVCD file is generated for CUT using conventional test patterns, and again iterated for CUT`s Fault Coverage upon applying conventional test vectors.

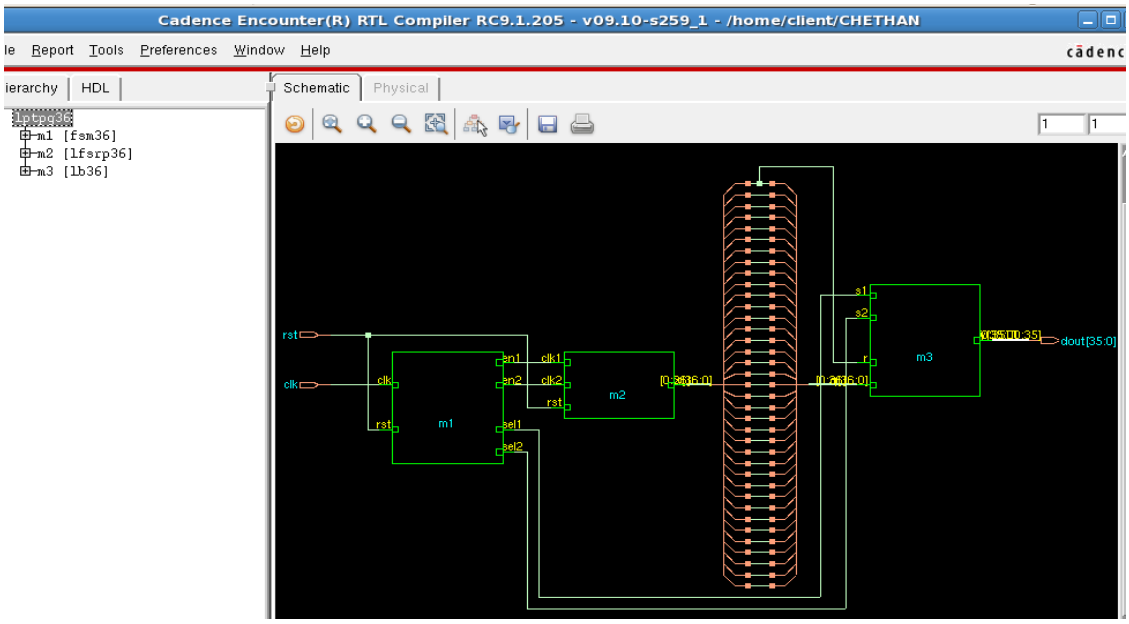

Figure 4: RTL schematic of low power Test Pattern Generator (TPG).

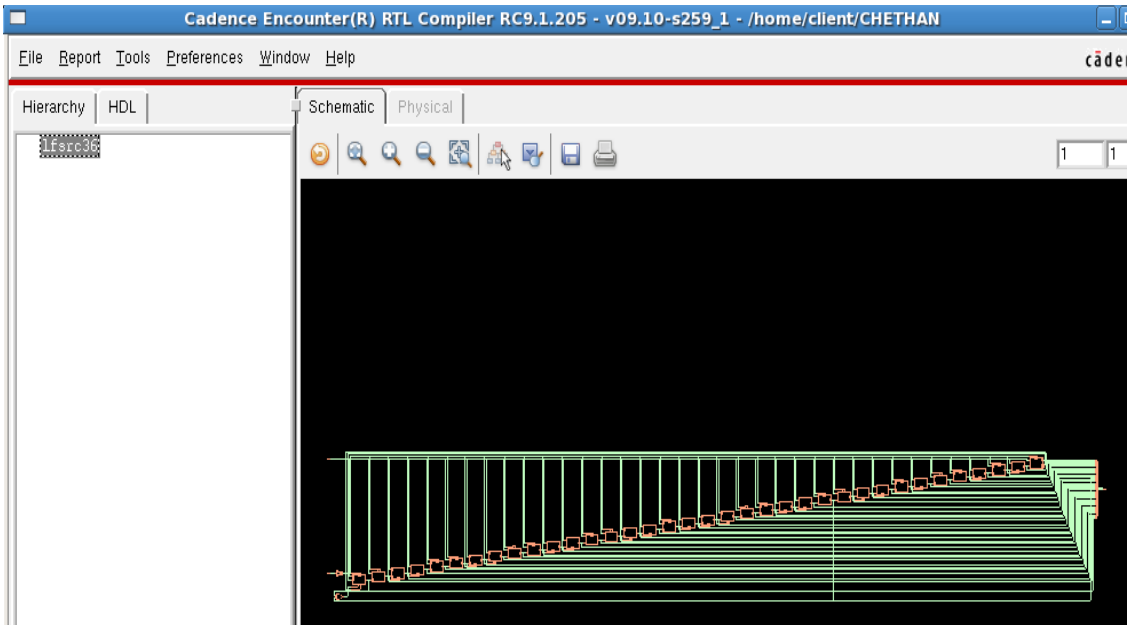

Figure 5: RTL schematic of standard LFSR.

5.1 Simulation and Power Results

The simulation waveforms validate the correct functionality of the 36 bit low power Test Pattern Generator (TPG) depicted fig. 6. The 36 bit wide patterns Generated by low power Test Pattern Generated (TPG) are shown below fig. 6. These 36 bit wide patterns are fed to the primary inputs of the Circuit Under Test (CUT) to detect the stuck-at faults inside the circuit under test.

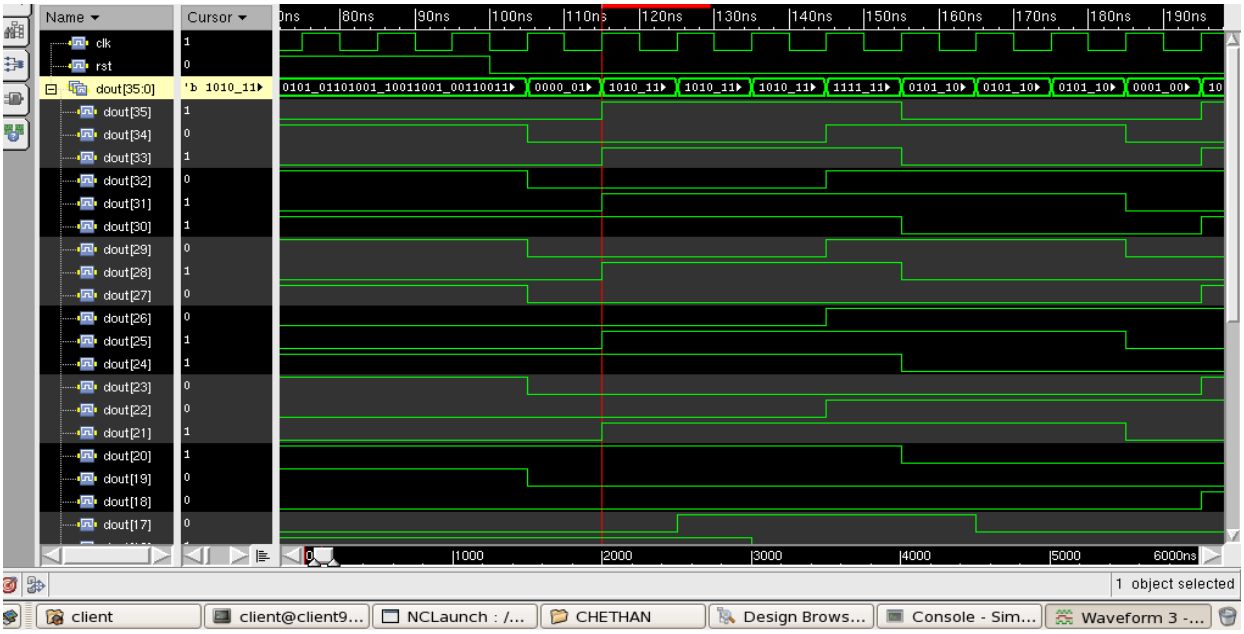

Figure 6: Simulation results of Low power Test Pattern Generator.

The reported power consumption estimation depicted in fig. 7 and fig. 8, that are the snapshots obtained after synthesis of the designs reveals that the power consumption of the low power Test Pattern Generator (TPG) is slenderized by 93% than compared to standard Linear Feedback Shift Register (LFSR). The comparison results of low power Test Pattern Generated (TPG) and Linear Feedback Shift Register (LFSR) are tabulated in table 2 which emphasizes significant reduction in the power consumed by low power Test pattern Generator than compared to Linear feedback shift Register.

```
File  Edit  View  Terminal  Tabs  Help

                    Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
-----------------------------------------------
lptpg36    192  3714.128  6155.991  9870.118
  m3       145  2280.460     0.000  2280.460
    u103     1    26.665     0.000    26.665
    u11      1    26.665     0.000    26.665
    u111     1    26.665     0.000    26.665
    u115     1    26.665     0.000    26.665
    u119     1    26.665     0.000    26.665
    u127     1    26.665     0.000    26.665
```

Figure 7: Power Consumption report of Low Power Test Pattern Generator

```
  Done mapping lfsrc36
  Synthesis succeeded.
rc:/> report power
================================================
  Generated by:           Encounter(R) RTL Compi
  Generated on:           Apr 04 2013  05:03:51 I
  Module:                 lfsrc36
  Technology library:     slow_normal 1.0
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================

                Leakage   Dynamic    Total
Instance Cells Power(nW) Power(nW) Power(nW)
------------------------------------------------
lfsrc36     38  1322.743 90247.672 91570.415
```

Figure 8: Power Consumption report of Standard LFSR.

Further the test vectors generated at the output of low power Test pattern Generator are deployed on CUT to dump Extended Value Change Dump (EVCD) file. This EVCD file consists of switching activity information of each and every node and nets of the Circuit Under Test (CUT). Thereafter generated EVCD file is read by the Automatic Test Pattern Generator (ATPG) tool as test vectors to test the CUT for stuck-at1 or stuck-at 0 faults in it. Similarly the above procedure is iterated for conventional Linear Feedback Shift Register outputs to obtain another (Extended Value Change Dump) EVCD file in order to test CUT using conventional LFSR test vectors.

Table 2: Comparison of Power consumption by low power Test Pattern Generator and standard Linear Feedback Shift Register

TPG	No. of cells	Dynamic Power consumption	% of reduction in power
36-bit standard LFSR	38	90.25 µW	N / A
36-bit Low Power TPG	192	6.15 µW	93%
16-bit TPG Proposed in [2]	76	10.22 µW	40%

The above depicted table 2 explains the comparison of power consumption of three test pattern generators (36 bit standard LFSR, 36 bit low power TPG and 16 bit Test pattern Generator). The comparative results reveals that standard LFSR utilizes lesser number of standard cells, but the dynamic power consumption by it is very high than compared to low power Test Pattern Generator. The low power Test Pattern Generator consumes more number of standard cells in its design but consumes very less power in operational mode.

Similarly the reported power consumption results indicated in table 3 below demonstrates approximately 82% lower power consumption by the Circuit Under Test (CUT) upon deploying low power test patterns than compared with the standard LFSR patterns. Even though the Circuit Under Test (CUT) consumes lesser number of conventional or the standard Linear Feedback Shift Register (LFSR) test vectors than compared to low powered one, to attain 100 percent fault coverage i.e. to detect all stuck-at faults in CUT, but it consumes more power inside CUT due to high switching activity. The Circuit Under Test consumes higher number low power test vectors derived from low power Test Pattern Generator (TPG), but it consumes less power in CUT than compared to conventional test vectors.

The tabulated results depicted in table 3 reveals the comparative study of examining the standard test vectors and low power test vectors. the CUT consumes 60 standard test vector to attain 100% fault coverage. The Circuit Under Test (CUT) consumes 45mWatt of power while computing for the desired fault coverage. Similarly in the second iteration the CUT uses 134 low power test vectors with just 8mWatt of power consumption. Hence 82% of CUT`s power is reduced while using low power test vectors than compared to standard test vectors This result reveals that lower number of logic transitions at the internal and external nodes of the Circuit under Test (CUT) which in turn reduces the switching activities inside it.

Table 3: Comparison of Power consumed by CUT on applying low power Test Pattern Generator and standard LFSR test vectors.

Applied Test Vectors	Standard LFSR Test Vectors	Low Power Test Vectors
NO. of Test Vectors utilized by CUT	60	134
NO. of gates in c432 (CUT)	160	160
Dynamic Power consumption by CUT	45mW	8mW
Total no. of cell faults in c432 (CUT)	86	86
Fault coverage	100%	100%
% of reduction in power	N / A	82%

VI. CONCLUSIONS

The proposed Test Pattern Generator (TPG) has been designed and implemented using EDA tools. The low power test patterns generated are composed of reduced number of bit flips between successive vectors which in turn reduced switching activities inside CUT and cent percent Fault Coverage (FC) is obtained by performing fault simulation of CUT. Hence the presented effective low power Test Pattern Generator consumes less power and also reduces the dynamic power consumed by CUT than compared to standard LFSR.

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Chethan J is a student pursuing post graduation. He graduated B.E. degree in Electronics and Communication Engineering from Siddaganga Institute of Technology, Tumkur in 2011. He is currently pursuing post graduation M.Tech degree in VLSI Design and Embedded Systems at VTU Extension Centre, UTL Technologies Ltd., Bangalore.

Manjunath Lakkannavar born in Dharwad, Karnataka in 1986. He received the B.E. degree in Electronics and Communication Engineering from SDMCET, Dharwad, Karnataka in 2008, and M.Tech degree in VLSI Design and Embedded Systems from KLECET, Belgaum, Karnataka in 2010. In 2010, he joined UTL Technologies Limited as Associate Consultant-VLSI department. His research interests are, VLSI Automation, Image Processing and Digital Communications, etc. He became a Guest of Honor and Session Chair for International Conference organized by InterScience Research Network (IRNet), Bhubaneshwar in 2012.

