

# Analysis and Design of Tri-Gate MOSFET with High Dielectrics Gate

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**Abstract**—The scaling of simple gate transistors requires the scaling and transistor elements like source/drain junction became difficult to scale further after a limit due to adverse effect of electrostatic and short-channel performance. The solution of the problem is tri-gate where we can increase the performance without increasing the width and without scaling. In this paper we have described the parameter of tri-gate and taking the high dielectric as substrate.

**Index Terms**—Tri-gate MOSFET; Radio frequency;  $\text{HfO}_2$ ; High dielectric constant; CMOS; VLSI.

## I. INTRODUCTION

A tri-gate transistor is an integrated transistor which consists of three gates before going to detailed analysis of tri-gate transistor let us have look the path to tri-gate transistor which covers the journey through double gate. The relationships between charge and potential are different for multi gate transistor and these cannot be mapped with classical junction based transistor hence these follows different modeling [1, 2]. The modeling of tri-gate transistor is quite different. *Sallese et. al.* [3] had modeled double gate in their publication and the model is valid in all regions of operation, from deep depletion to accumulation and from linear to saturated regimes. *Srivastava et. al.* [4] has discussed that the double-gate MOSFETs provides good scalability and better immunity to short channel effects, these can overcome the era of CMOS. *Sarkar et. al.* [5] has developed a model for the noise parameter such as power spectral density and noise figure can be improved with the help of technologies in good extent. The increased electron mobility and velocity at channel surface due to dual gate material reduce effective electrical field at drain end, resulting in smaller DIBL and hot carrier effects [6]. *Taur et. al.* [7] has presented an explicit continuous models are used for double-gate and surrounding-gate (tri-gate) with no loss of physics. These models inherit all the favorable features from those models, which have been verified. *Srivastava et. al.* [8] have presented a design and performance analysis of cylindrical surrounding double-gate MOSFET which

is an advanced version of the Tri-gate, used for the purpose of RF switches.

A tri-gate transistor is an integrated transistor which consist three gates arranged around the three phases of substrate in such a manner that cover the three of four sides (top, side 1, side 2 and bottom). Side 1, side 2, and top are acquired by the gate-1, gate-3, and gate-2 respectively. Gate-3 has physical length  $L$  and width  $W$  while gate-1 and gate-2 has the length  $L$  and width  $H$  as shown in the fig. 1.

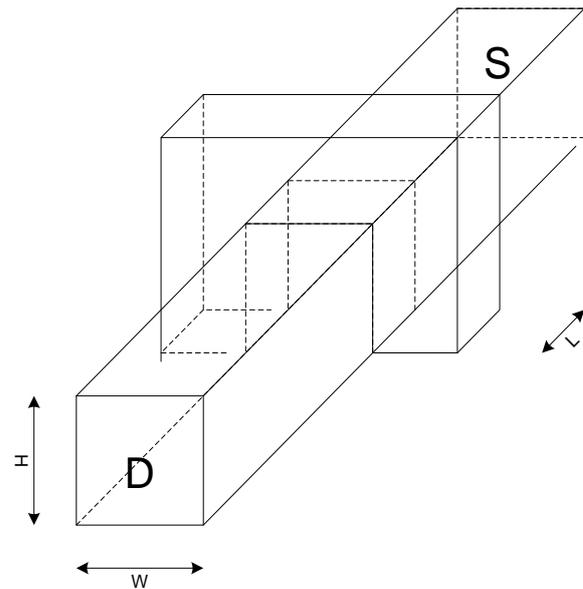


Figure 1. Structure of tri-gate transistor.

The technology is changing rapidly to keep pace with Moore's law for that the cell size is reduced more and more scaling of transistors have been done for better packing on chip. But parasitic leakage creates a problem with scaling due to worsening short channel effect. While in tri-gate transistor the short channel effect improved considerably. Tri-gate transistor design utilize low aspect ratio channel to provide evolutionary pathway for CMOS scaling to the end of roadway [9-11]. The design provides the advantages of multi-gate transistor with the advantage of planner MOSFET. Tri-Gate body dimensions are flexible as compared to single

gate double and gate transistors and also the plays an important role in determining V-I characteristics [12, 13]. By applying stress memorization techniques we can achieve considerable on-current improvement. As the short channel performance are given by the ratio of  $W/L$ . In tri-gate transistor it is given by the ratio of  $(W+2H)/L$ . Because the total drives current of the tri-gate transistor is a function of addition of gate-1, gate-2 and gate-3 that is depending on cumulative effect of H, W and H. Hence it is given by  $(W+2H)$  over L and not by W over L as in simple transistor. This clearly shows if we increase the height of transistor we will get more drive current.

## II. MODELLING OF TRI-GATE MOSFET

The drain to source current in any transistor is proportional to  $W/L$  ratio and depends upon the oxide capacitance and the value of the mobility of the majority carriers. In any normal transistor the drain to source current is defined by the equation:

$$I_{ds} = \left(\frac{W}{L}\right) \left(\frac{\mu C_{ox}}{2}\right) [2(V_{gs} - V_t)V_{ds} - V_{ds}^2] \quad (1)$$

Where  $I_{ds}$  is the drain to source is current,  $C_{ox}$  is oxide capacitance,  $\mu$  is mobility of electrons,  $V_{ds}$  drain to source voltage,  $V_{gs}$  is gate to source voltage and  $V_t$  is threshold voltage of transistor.

The drain to source current in tri-gate transistor is proportional to  $\frac{W+2H}{L}$  ratio. Here H is the width of the transistor and drain to source current is given by the equation:

$$I_{ds} = \left(\frac{W+2H}{L}\right) \left(\frac{\mu C_{ox}}{2}\right) [2(V_{gs} - V_t)V_{ds} - V_{ds}^2] \quad (2)$$

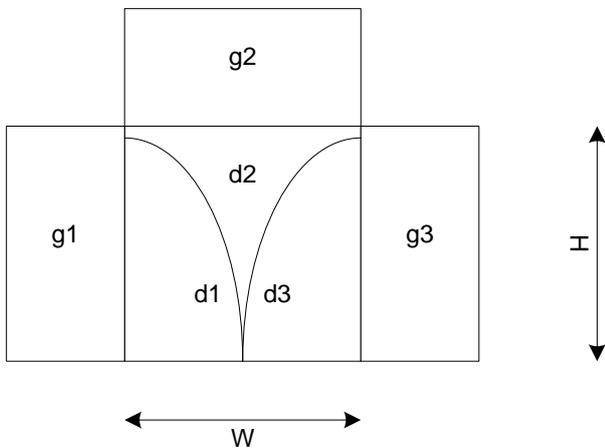


Figure 2. Transverse view of tri-gate transistor.

Here the current will be increased because the  $W/L$  ratio is improved due to addition of  $2H$  and hence

current characteristics will be improved. Now take the mobility electron in Gallium Arsenide  $\mu = 8500 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  [5], the oxide capacitance  $C_{ox} = 10.588 \text{ nF}$ , then the value of  $\mu C_{ox} = 90 * 10^{-6} \text{ A/V}^2$ , the gate length of transistor is  $L = .045 \text{ }\mu\text{m}$  and height  $H = 5 \text{ }\mu\text{m}$ . Suppose the threshold voltage for transistor  $V_t = 0.6 \text{ V}$  and the gate to source voltage  $V_{gs} = 1 \text{ V}$ ,  $2 \text{ V}$  and  $3 \text{ V}$ , then the equation for the drain to source current for normal gate transistor  $I_{ds}$  will be given by the Equation (1) and taking the width of the gate of the transistor  $W = 22.5 \text{ }\mu\text{m}$ .

$$I_{ds} = 22.5[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 22.5[0.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 1 V.

$$I_{ds} = 22.5[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 22.5[2.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 2 V.

$$I_{ds} = 22.5[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 22.5[4.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 3 V.

Now taking another value of width of the gate of the transistor which is higher with respect to the earlier value that is  $W = 90 \text{ }\mu\text{m}$  and calculating the value of drain to source current according to equation (1).

$$I_{ds} = 90[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 90[0.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 1 V.

$$I_{ds} = 90[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 90[2.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 2 V.

$$I_{ds} = 90[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 90[4.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 3 V.

Further we have analyze the value of drain to source current  $I_{ds}$  for tri-gate transistor for which the drain to source current will be given by the Equation (2). The only change for tri-gate transistor will be the improvement provided by the height of the gate of transistor that is  $2H = 10 \text{ }\mu\text{m}$ . We analyzed the results for the same values of parameters which we have chosen for the normal transistor and the width of the gate of the tri-gate transistor  $W = 22.5 \text{ }\mu\text{m}$ .

$$I_{ds} = 32.5[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 32.5[0.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 1 V.

$$I_{ds} = 32.5[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 32.5[2.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 2 V.

$$I_{ds} = 32.5[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 32.5[4.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 3 V.

Now taking another value of width of the gate of the transistor which is higher with respect to the earlier

value that is  $W = 90 \mu\text{m}$  and calculating the value of drain to source current according to Equation (2).

$$I_{ds} = 100[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 100[0.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 1 V.

$$I_{ds} = 100[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 100[2.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 2 V.

$$I_{ds} = 100[2(V_{gs} - V_t)V_{ds} - V_{ds}^2] = 100[4.8V_{ds} - V_{ds}^2]$$

In the above equation we have to put the value of drain to source voltage ( $V_{gs}$ ) = 3 V.

### III. SIMULATION RESULT OF TRI-GATE MOSFET

From here we can see that the improvement for small dimensions is considerably greater than large dimensions for larger dimension the drain to source current is 1.1 times of simple gate transistor value but for smaller dimensions the drain to source current is 1.44 times of simple gate transistor value for same width. The simulated MATLAB graphs are shown in the figures.

For smaller dimensions we can see in the graph as in Fig. 4. When the value of drain to source voltage ( $V_{ds}$ ) is 0.74 V at 4 V gate to source voltage ( $V_{gs}$ ) the corresponding values of  $I_{ds}$  in simple gate transistors and tri-gate transistors are 100 mA and 144 mA and for larger dimensions when the value of drain to source voltage ( $V_{ds}$ ) is 0.8 V at 3 V gate to source voltage ( $V_{gs}$ ) the corresponding values of drain to source current ( $I_{ds}$ ) in simple gate transistors and tri-gate transistors are 288 mA and 320 mA.

Now let us analyze the tri-gate with another material [14, 15]. We will take the  $\text{HfO}_2$  for our analysis and will compare it with gallium arsenide. Since the graph of the mobility of electron in  $\text{HfO}_2$  ranges from 325 to 375, so taking the approximated value of the mobility we choose the value 350. That means  $\mu = 350$  and all other parameter and condition will remain same.

After calculating the values of drain to source current ( $I_{ds}$ ) for different values of width of the gate (W) for 45nm technology for all previous values of gate to source voltages ( $V_{ds}$ ) for tri-gate transistor as well as normal transistor are shown in table 1.

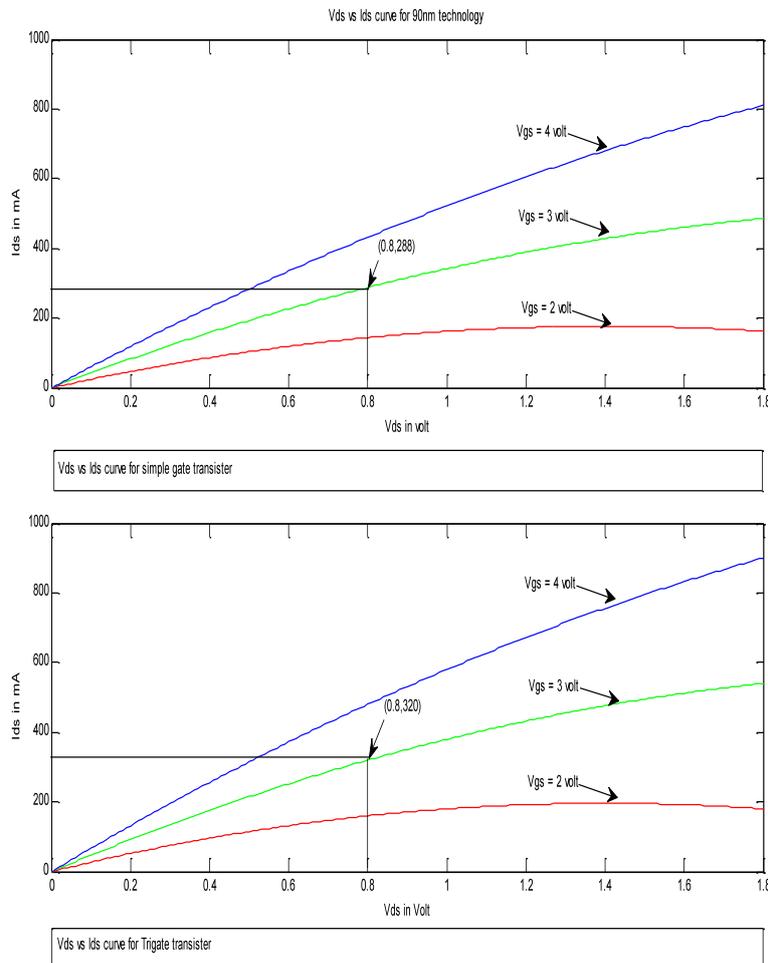


Figure-3 Simulated result for simple and tri-gate transistor the width of gate  $W = 90 \mu\text{m}$ .

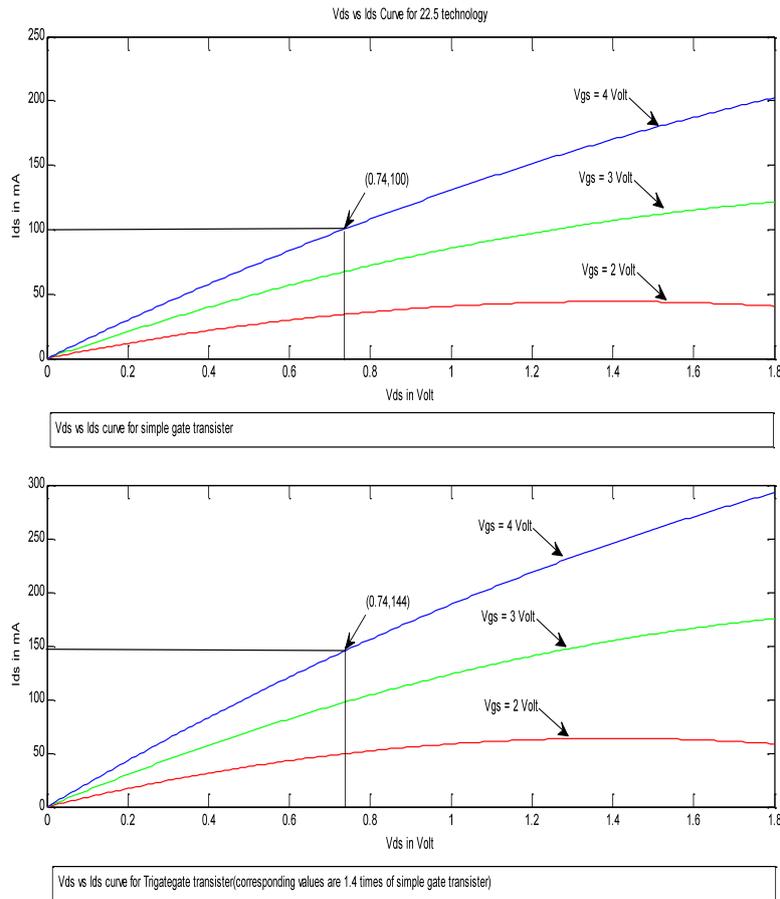


Figure 4. Simulated result for simple and tri-gate transistor the width of gate  $W = 20 \mu\text{m}$ .

TABLE 1. VALUES OF  $I_{D,s}$  (DRAIN TO SOURCE CURRENT) FOR  $\text{HfO}_2$

Type of transistor	W( $\mu\text{m}$ )	$V_{gs}$ (Volt)	$I_{ds}$ (mA)
Normal	22.5	1	$0.926[0.8V_{ds} - V_{ds}^2]$
		2	$0.926[2.8V_{ds} - V_{ds}^2]$
		3	$0.926[4.8V_{ds} - V_{ds}^2]$
	90	1	$3.705[0.8V_{ds} - V_{ds}^2]$
		2	$3.705[2.8V_{ds} - V_{ds}^2]$
		3	$3.705[4.8V_{ds} - V_{ds}^2]$
Tri-gate	22.5	1	$1.338[0.8V_{ds} - V_{ds}^2]$
		2	$1.338[2.8V_{ds} - V_{ds}^2]$
		3	$1.338[4.8V_{ds} - V_{ds}^2]$
	90	1	$4.118[0.8V_{ds} - V_{ds}^2]$
		2	$4.118[2.8V_{ds} - V_{ds}^2]$
		3	$4.118[4.8V_{ds} - V_{ds}^2]$

TABLE-2 VALUES OF  $I_{ds}$  (DRAIN TO SOURCE CURRENT) FOR COMPARISON BETWEEN GAAS AND HfO<sub>2</sub>.

Material	Type of transistor	W( $\mu$ m)	V <sub>gs</sub> (Volt)	I <sub>ds</sub> (mA)
HfO <sub>2</sub>	Normal	22.5	1	$0.926[0.8V_{ds} - V_{ds}^2]$
			2	$0.926[2.8V_{ds} - V_{ds}^2]$
			3	$0.926[4.8V_{ds} - V_{ds}^2]$
		90	1	$3.705[0.8V_{ds} - V_{ds}^2]$
			2	$3.705[2.8V_{ds} - V_{ds}^2]$
			3	$3.705[4.8V_{ds} - V_{ds}^2]$
	Tri-gate	22.5	1	$1.338[0.8V_{ds} - V_{ds}^2]$
			2	$1.338[2.8V_{ds} - V_{ds}^2]$
			3	$1.338[4.8V_{ds} - V_{ds}^2]$
		90	1	$4.118[0.8V_{ds} - V_{ds}^2]$
			2	$4.118[2.8V_{ds} - V_{ds}^2]$
			3	$4.118[4.8V_{ds} - V_{ds}^2]$
GaAs	Normal	22.5	1	$22.5[0.8V_{ds} - V_{ds}^2]$
			2	$22.5[2.8V_{ds} - V_{ds}^2]$
			3	$22.5[4.8V_{ds} - V_{ds}^2]$
		90	1	$90[0.8V_{ds} - V_{ds}^2]$
			2	$90[2.8V_{ds} - V_{ds}^2]$
			3	$90[4.8V_{ds} - V_{ds}^2]$
	Tri-gate	22.5	1	$32.5[0.8V_{ds} - V_{ds}^2]$
			2	$32.5[2.8V_{ds} - V_{ds}^2]$
			3	$32.5[4.8V_{ds} - V_{ds}^2]$
		90	1	$100[0.8V_{ds} - V_{ds}^2]$
			2	$100[2.8V_{ds} - V_{ds}^2]$
			3	$100[4.8V_{ds} - V_{ds}^2]$

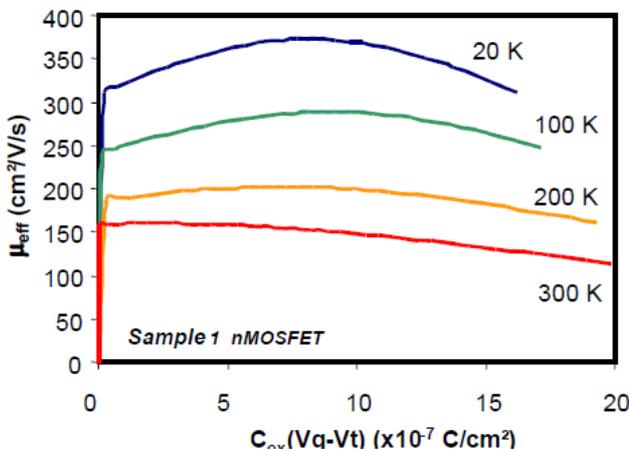


Figure 5. Variation in mobility of electron in HfO<sub>2</sub> with the difference of gate to source voltage and threshold voltage [5].

IV. RESULTS AND CONCLUSIONS

We have compared the results of Hafnium dioxide and Gallium Arsenide in same condition then we find the only difference in mobility of electrons in the materials. Which affects the result considerably and the Hafnium dioxide has lesser value of mobility hence gives lower value of drain to source current. The table 2 shows the comparison of the values of drain to source current in both the cases Hafnium dioxide as well as Gallium Arsenide.

Now if we compare between tri-gate transistor with simple transistors results then for the value of greater width ( $W = 90 \mu$ m) of the transistor the improvement in tri-gate transistor with respect to normal transistor is just only 1.13 time of the simple transistor's value but for the smaller width ( $W = 22.5 \mu$ m) of the transistor the improvement in tri-gate transistor with respect to normal transistor is 1.44 time which can be verified by the

table 2 and as well as by the simulation results. From this table, if we consider the case of GaAs with 2 V gate to source voltage ( $V_{gs}$ ) of width  $W = 90 \mu m$  then improvement is *1.13 times* of normal transistor while it is *1.44 times* of the normal values in case of width  $W = 22.5 \mu m$ .

In the proposed tri-gate transistor we achieved a better performance without scaling, as scaling of simple transistors need to scale the oxide and junctions. Scaling became problematic after a certain limit because electrostatics and short channel performance getting worse as the gate length is reduced after a limit. Thus scaling provides limits over it and we cannot scale the dimensions as we desire. Since we have to deal with electrostatics and short channel performance, hence we need a technology which do not apply scaling for improvement and that is done in tri-gate. After analyzing the tri-gate we can use this for the purpose of double-pole four-throw RF switch design [16].

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