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Optical Packet Switch Architectures: A Comparative Study

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***Abstract*—** In this paper four fiber-loop-buffer based photonic packet switched architectures are compared. It is done in terms of their packet loss probability and their optical cost under various load conditions for the random traffic model. The recirculating type delay lines are used for the storage of packets to resolve the contention. The architectures use semiconductor optical amplifiers(SOAs) and tunable wavelength converters(TWCs) in the recirculating loop buffer. The architectures have advantage of simultaneous Read/Write and, wavelength reallocation using TWCs in the recirculating loop buffer. Therefore, it improves the switch performance over the architectures using SOAs in the loop buffer. The cost of the various architectures is evaluated by considering FCC (fiber-to-chip coupling) and the WSU (wavelength speed up factor) model.

***Index Terms*—** Photonic Packet Switching, Packet Loss Probability, Optical Cost, Load

I. Introduction

The photonic packet switching[1] appears to be a strong candidate among all the switching schemes, because of its high speed. The concept of wavelength division multiplexing (WDM) has provided an opportunity to multiply the network capacity. WDM systems allow the utilization of the higher bandwidth of the fiber by transmitting multiple signals on a single fiber [2]. The contention among the packets is one of the major drawbacks in optical switching. In the network switches when two or more packets have to exploit the same resources contentions comes in to picture [3]. A solution to this problem is optical buffering [4]. which is implemented using a set of Fiber Delay Lines (FDL) [5 ,6 ,7 ,8 ,9 ,10 ,11 ,12 ,13 ,14] . The FDL delays an incoming packet for a specific amount of time. The delay is proportional to the length of the fiber. The recirculating-type delay lines are more flexible because storage time is adjustable by changing the circulating number. The number of fiber delay lines used in any architecture can be reduced by using wavelength conversion. In this paper the cost of different architectures are given using two different models. The architectures are compared in terms of their optical cost and packet loss probability.

This paper is organized as follows: Section 2 gives structure of optical packet switched networks Section 3 describes the related work. Section 4 presents the cost analysis of the optical packet switch architectures. Results and conclusions are given in the final section.

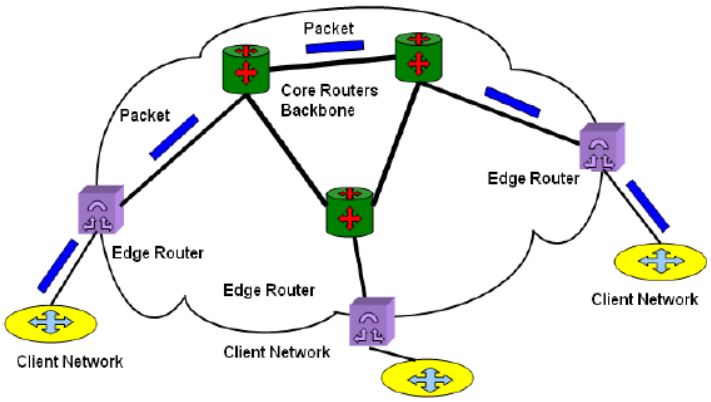

Fig. 1: Schematic of the generalized optical networks

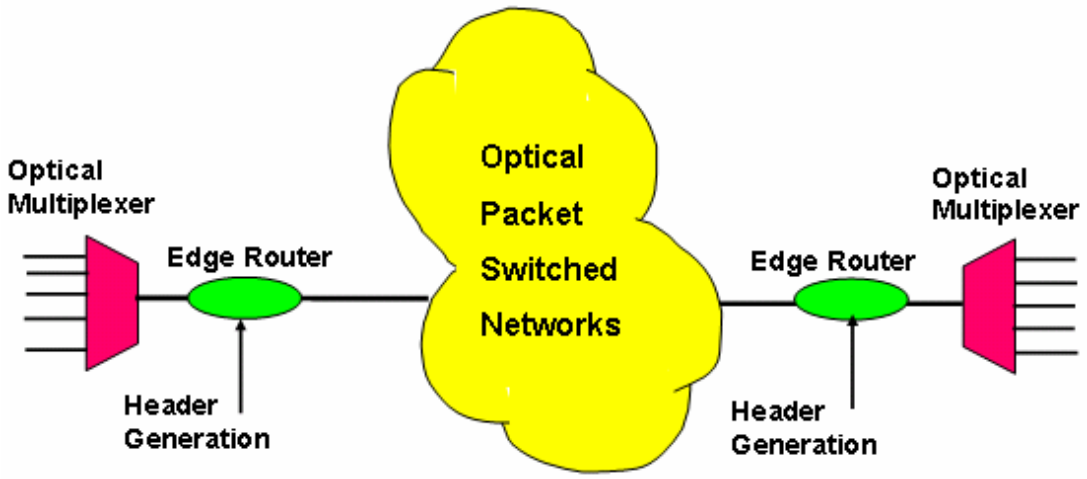

Fig. 2: Schematic of the aggregated core networks

II. Structure of Optical Packet Switched Networks

The generic layout of the network is shown in Figure 1. The edge routers acting as an interface between clients and core network lie on the periphery of the network cloud. Core as well as edge routers are electronic in nature. It is not possible to handle high data rate with these electronic routers hence, possessing speed limitations. To overcome this problem aggregate core transport networks as shown in Figure 2 came in to picture. The packet header is processed electronically at a slower rate, while the payload is processed optically at a higher rate [15] . The motivation to build the optical packet switch is when ingress node (edge router) aggregate the large number of packets optically for a very high bit rate payload, as the data is generated by the electronic sources. The switch in the core network will convert the low bit rate header of the packet (attached with a high bit rate payload) in electronic domain and maintains the payload in optical form. Routing of the packet is done as per the information stored in the header. The aggregated packet can be separated optically and passed in to the client network as soon as it reaches the egress node i.e. the edge router at which packet exists the core network.

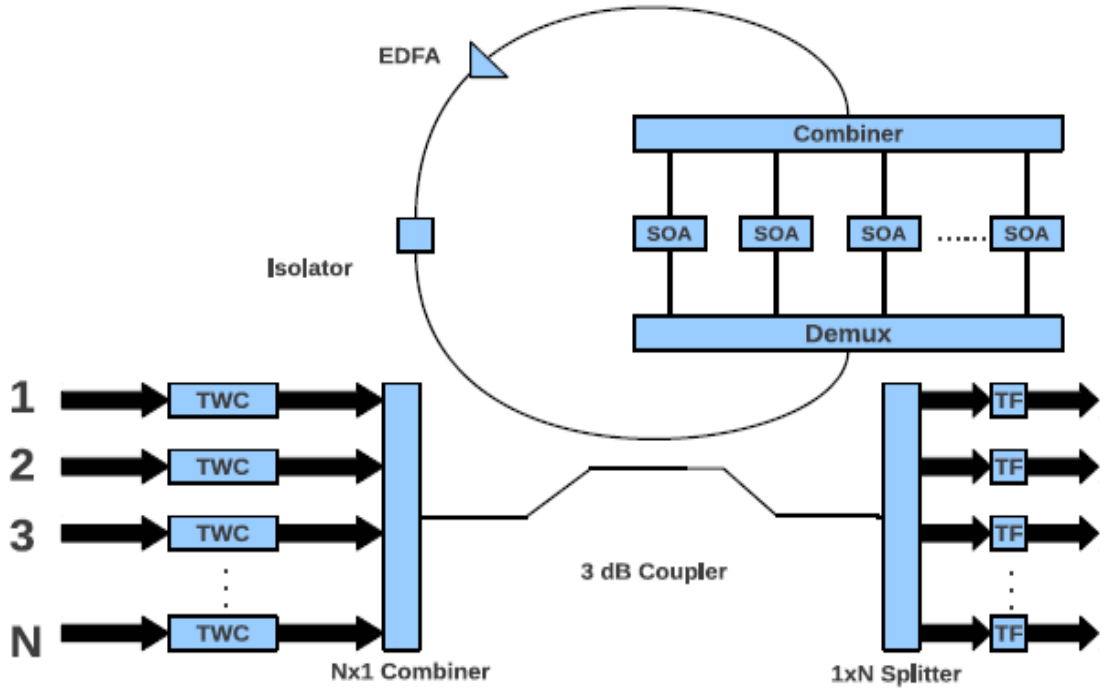

Fig. 3: Schematic of loop buffer architecture A1

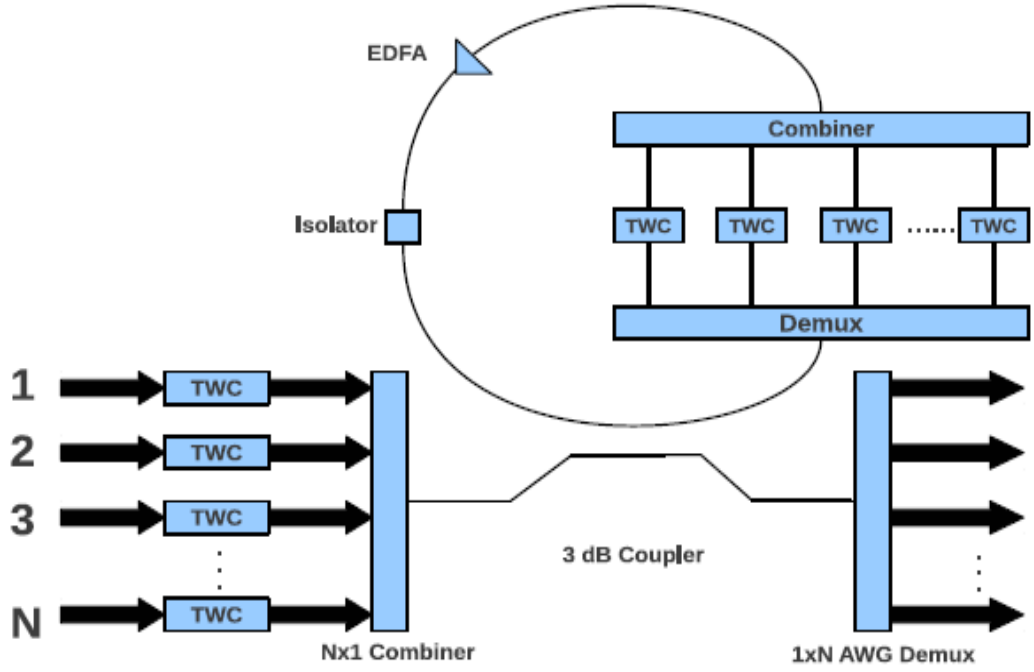

Fig. 4: Schematic of loop buffer architecture A2

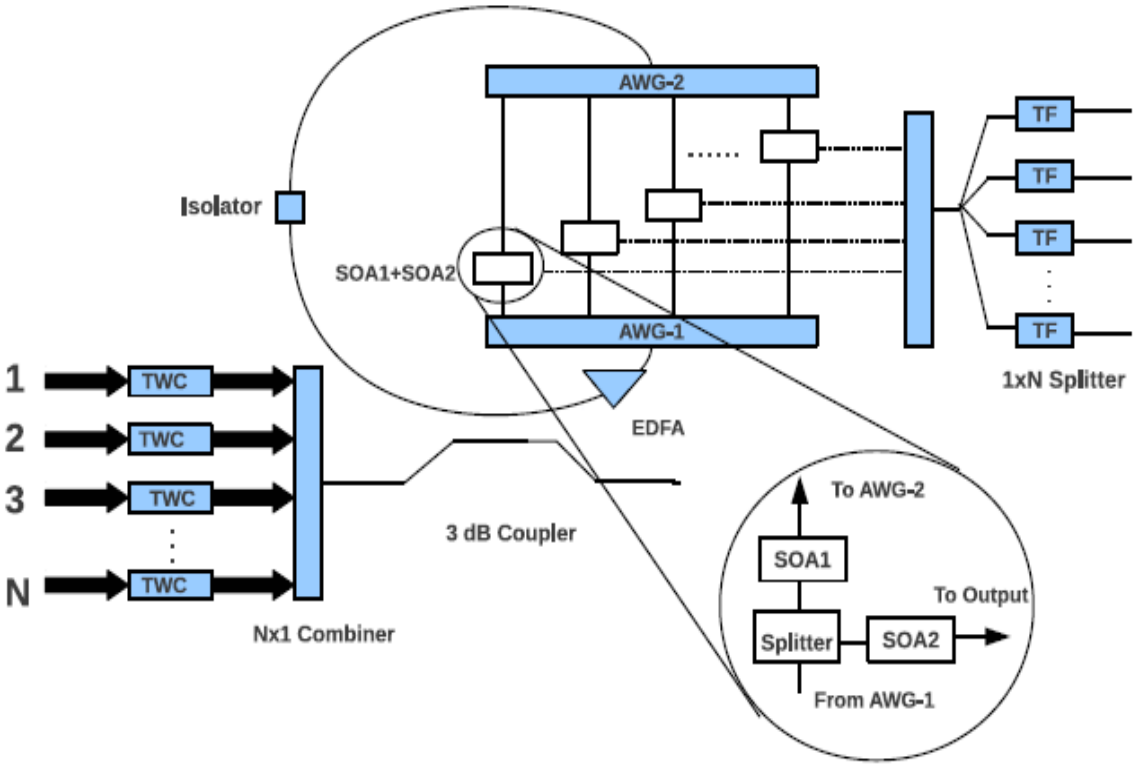

Fig. 5: Schematic of loop buffer architecture A3.

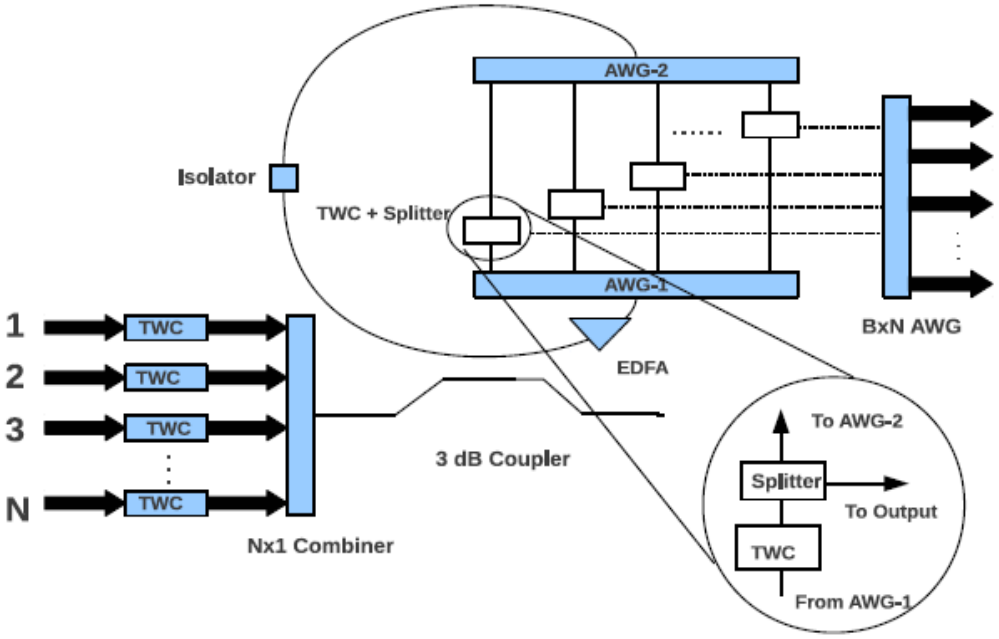

Fig. 6: Schematic of loop buffer architecture A4

III. Related Work

The switch architectures (A1-A4) are shown in Figure 3-6 [16]. They consist of *N* TWCs, one at each input. The TWCs are tuned in every time slot to appropriate wavelength to place a packet in the loop buffer for avoiding contention. The Architecture A1 (Figure 3) proposed by Bendelli *et al.* [7] has SOA as gate switches in recirculating loop buffer for a specified number of wavelengths. The architecture A2 (Figure 4) proposed by Srivastava *et al.* [9] contain tunable wavelength convertors (TWCs) inside the buffer, which can resolve contention among the packets in wavelength domain. The architecture A3 was proposed by Choa *et al.* [12]. In A3 demux and combiner used in buffer loop of A1 and A2 are replaced by AWG demultiplexer (AWG-1) and AWG multiplexer(AWG-2). Two SOA gates are placed in each branch of the AWGs of the buffer. Figure 6 depicts the architecture proposed in [16]. All the architectures are designed for equal length packets. The packets are assumed to be frame aligned when they arrive at the input of the switch [17]. These architectures use recirculating-type delay lines for the storage of packets.

These four architectures can be compared in terms of their functionalities as :

1. Simultaneous read/write: The writing of a new packet can take place simultaneously as a packet from the buffer is being readout. Architecture A2 and A4 supports simultaneous read-write whereas architecture A1 and A3 does not support simultaneous read-write operations(as seen from Figure 3).
2. Wavelength reallocation: Buffering is used for contention resolution. Storage time can be adjusted by changing the number of circulations. However there is a limit on the maximum number of circulations [18]. One of the factors responsible for this limit is cross talk. To reduce the noise due to cross talk dynamic wavelength reallocation is used which result in an increase in maximum buffering time. This wavelength conversion also reduces packet loss probability [19]. To minimize cross talk in DWDM networks TWCs has been used as buffer gates. This is possible in architectures A2 and A4 only.
3. Control complexity: It does the processing of routing information, updates header information, forwards header to output interface, tracking buffer and input-output port status, synchronization of operation of switch components with master clock in reference, communication with other switching nodes etc. It is implemented electronically and the actual data transmission takes place optically. It depends on the photonic components requiring synchronized control. In architectures A2 and A4 only two components, input and buffer TWCs, have to be controlled so it's control complexity is lowest. The control complexity of the architectures A2 and A4 is lowest as only two components, input and buffer TWCs, have to be controlled. For architecture A1,three components-the input TWCs, buffer SOAs, and output TFs have to be controlled, so it's control unit complexity is moderate. . In architecture A3 four components, i.e., input TWCs, two buffer SOAs, and TFs at the output have to be

controlled by the control unit, so the control unit complexity is very high.

4. Number of components: The cost of architectures depends on the number and type of components. The physical loss in the architectures can also be calculated by considering the insertion loss of each device. Number of components are lowest in architecture A2 and highest for architecture A3.

5. Buffer utilization: Buffering is used for contention resolution. Optical buffer is one of the critical component of optical packet switching. Current optical buffers are mainly based on fiber delay lines which delay the packets rather than to store them.

6. For the architectures A1 and A2 the buffer capacity (*B*) can be fully utilized, but for the architectures A3 and A4, the buffer capacity is shared by the directly transmitted and buffered packets. Between the architectures A1 and A2, the latter utilizes the buffer capacity more effectively, as for this architecture simultaneous read-write operation is possible that is not possible for the architecture A1.

7. Packet loss probability: Packet loss is the failure of one or more transmitted packets to arrive at their destination.

Considering the Random Traffic Model, packet loss probability for the switch configuration , under various load conditions has been examined using computer simulation. In Figure 7 packet loss probability versus load on the system is plotted for different buffer architectures for the random traffic model [16] .

Further the architectures can also be compared in terms of their Packet loss probability and cost. In the cost analysis of the architectures two models have been considered namely fiber-to-chip coupling (FCC) and wavelength speed-up model (WSU).

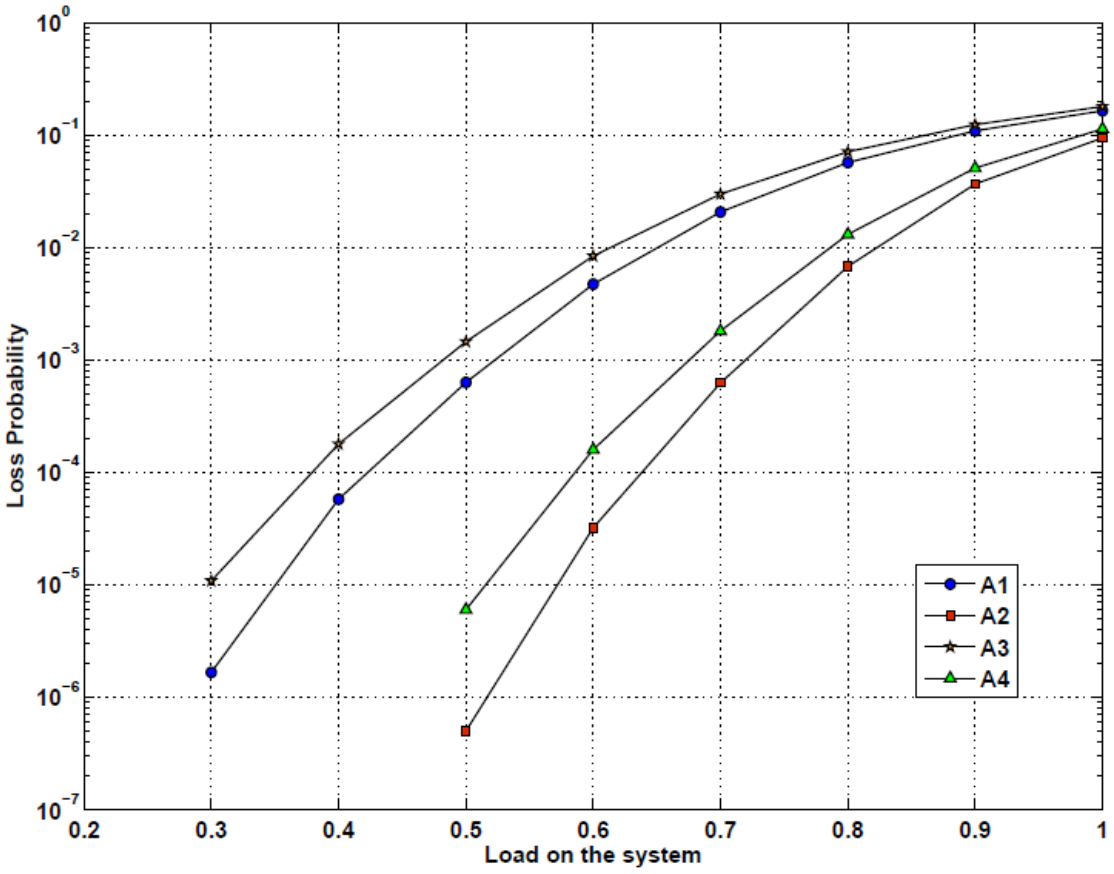

Fig 7: Packet loss Probability versus Load

IV. Cost Analysis of the Optical Packet Switch Architectures

In this paper four optical packet switch architecture have been discussed. These architectures have their advantages over the other. One of the most important issue is the cost of these architectures. The, cost estimation of the architecture is not straight forward. The first compact model which is helpful in the estimation of the cost of the architectures was proposed by Caenegem [20]. The proposed cost model is based on fiber-to-chip coupling (FCC) which is the number of

interconnections to the outer world through the component, where the cost of optical components is obtained by counting the number of FCC. The model assumes fix cost for the passive and active devices. Therefore, the cost of the optical components can be written as,

$$C_{opticaldevice} = Input\ fibers + Output\ fibers \quad (1)$$

Thus, cost of the TWC which can be tuned to W wavelengths is assumed to be 4 (3 input fiber + 1 output fiber). The optical cost of the various devices in terms of FCC is presented in Table 1

Table 1: Optical cost of the various devices using FCC method

Symbol	Representation	Cost
C_{TWC}	Cost of the TWC	4
$C_{Combiner}^{N\times1}$	Cost of the Combiner	N+1
$C_{Splitter}^{N\times1}$	Cost of the Splitter	N+1
C_{3dB}	Cost of 3 dB Coupler	4
$C_{Demux}^{N\times1}$	Cost of the Demux	N+1
$C_{Mux}^{N\times1}$	Cost of the Mux	N+1
C_{EDFA}	Cost of the EDFA	2
C_{ISO}	Cost of the Isolator	2
$C_{\mathrm{Re}ge}$	Cost of the Regenerator	21
C_{SOA}	Cost of the SOA	2
C_{FBG}	Cost of the FBG	2
$C_{AWG}^{N\times\mathrm{N}}$	Cost of the AWG	2N
C_{FF}	Cost of the FF	2
C_{TF}	Cost of the TF	2
C_{Cir}^{N}	Cost of the Circulator	N
C_{F}	Cost of the Fiber	2
C_{Or}	Cost of the Optical reflector	2

As this model assumes fixed cost, this model does not include the wavelength speed-up factor (WSU). To incorporate the effect of wavelength conversion, a heuristic cost model is proposed in [21] where the cost of the TWC's is given by the expression

$$C_{TWC} = ah \quad (2)$$

Here, a is a normalization constant, h is the conversion range. Thus, the cost of the TWC which can be tuned to W wavelengths will be given by,

$$C_{TWC} = aW \quad (3)$$

The model assumes linear trend in cost with respect to the tunable wavelength range. In [22] , a relatively more generalized model have been presented where cost is given as,

$$C_{TWC} = ah^b \quad (4)$$

Where, a is a normalization constant, h is the conversion range and b is wavelength speed-up characterization parameter which characterizes the cost of the TWC and its values lies between 0.5 to 5. The cost of the TWCs which can be tuned to wavelengths will be given by,

$$C_{TWC} = \begin{cases} aW^b, & W > 1 \\ a, & W = 1 \end{cases} \quad (5)$$

As per the cost model presented in [22] the maximum possible value of a is one. Therefore, TWCs which can tune to one wavelength only will cost unity. The cost model is further modified by considering the concept of LRWC (limited range wavelength converter) and FRWC (full range wavelength converter) and it is concluded that the value of the speed up factor should be in between 0.5 and 1. Further detailing can be found in [23].

4.1 Cost Estimation of the Architectures

In this section, optical cost of various architectures is computed. The total costs of the various architectures are computed by counting the cost of the all the devices needed to realize each switch structure. The cost of different architectures is computed by breaking the each architecture in three separate units as input, buffer and output where the cost of each unit will be given as C_{in} C_{loop} and C_{out} respectively. The cost of the architecture A1 can be computed as,

The cost of the input unit which consists of TWCs and combiner can be written as,

$$C_{in} = NC_{TWC}^{in} + C_{Com}^{N\times1} \quad (6)$$

The cost of the output unit which consists of splitter and tunable filter will be given by,

$$C_{out} = C_{Splitter}^{1\times N} + NC_{TF} \quad (7)$$

Similarly, the cost of the buffer unit will be given by,

$$C_{loop} = C_{3dB} + C_{Demux}^{1\times B} + BC_{SOA} + C_{Com}^{B\times1} + C_{EDFA} + C_{ISO} + C_{F} \quad (8)$$

In the notation, cost of each component is represented as C_p^q where p shows the component type and q is size/position of the device. In the subsequent cost equations buffer is represented as bu. Similarly, the costs of the architecture A2 can be modeled as,

$$C_{in} = NC_{TWC}^{in} + C_{Com}^{N\times1} \quad (9)$$

$$C_{out} = C_{Demux}^{1\times N} \quad (10)$$

$$C_{loop} = C_{3dB} + C_{Demux}^{1\times B} + BC_{TWC}^{bu} + C_{Com}^{B\times 1} + C_{EDFA} + C_{ISO} + C_F \quad (11)$$

The costs of the architecture A3 is given by the expression,

$$C_{in} = NC_{TWC}^{in} + C_{Com}^{N\times 1} \quad (12)$$

$$C_{out} = C_{Demux}^{1\times N} + C_{Splitter}^{1\times N} + NC_{TF} \quad (13)$$

$$C_{loop} = C_{3dB} + C_{EDFA} + C_{Demux}^{1\times B} + B(C_{Splitter}^{1\times 2} + 2C_{SOA}) + C_{Mux}^{B\times 1} + C_{ISO} + C_F \quad (14)$$

The costs of the architecture A4 can be expressed as,

$$C_{in} = NC_{TWC}^{in} + C_{Com}^{N\times 1} \quad (15)$$

$$C_{out} = C_{Demux}^{B\times N} + NC_{TF} \quad (16)$$

$$C_{loop} = C_{3dB} + C_{EDFA} + C_{Demux}^{1\times B} + B(C_{TWC}^{bu} + C_{Splitter}^{1\times 2}) + C_{Mux}^{B\times 1} + C_{ISO} + C_F \quad (17)$$

The optical costs of the different components using FCC methods are tabulated in Table 1. After applying the cost of the different components the cost of the various architectures will be given by the expressions,

$$C_{A1} = NC_{TWC}^{in} + 4N + 4B + 14 \quad (18)$$

$$C_{A2} = NC_{TWC}^{in} + BC_{TWC}^{bu} + 2N + 2B + 2B + 14 \quad (19)$$

$$C_{A3} = NC_{TWC}^{in} + 4N + 10B + 15 \quad (20)$$

$$C_{A4} = NC_{TWC}^{in} + BC_{TWC}^{bu} + 4N + 6B + 11 \quad (21)$$

In the next two sections cost of the architecture are evaluated numerically, by considering N=4 and B=8 using the two models.

4.2 Cost of the Architectures using FCC Method

In Figure 8, the costs of the architectures are evaluated by considering FCC model. The cost of the TWC is assumed to be 4 which is independent of the tunable range of the TWCs. Here the cost of the architecture A3 is highest (127 units). The cost of the architecture A3 and A4 is comparable to each other similarly the cost of A1 and A2 is comparable to each other. The FCC cost model does not take into account of tunable range of the TWCs, therefore higher cost of the architecture can be considered as direct measure of the number of components or size of the components to realize the switch architecture. It should be noted that more number of components with larger switch size will add to the cost.

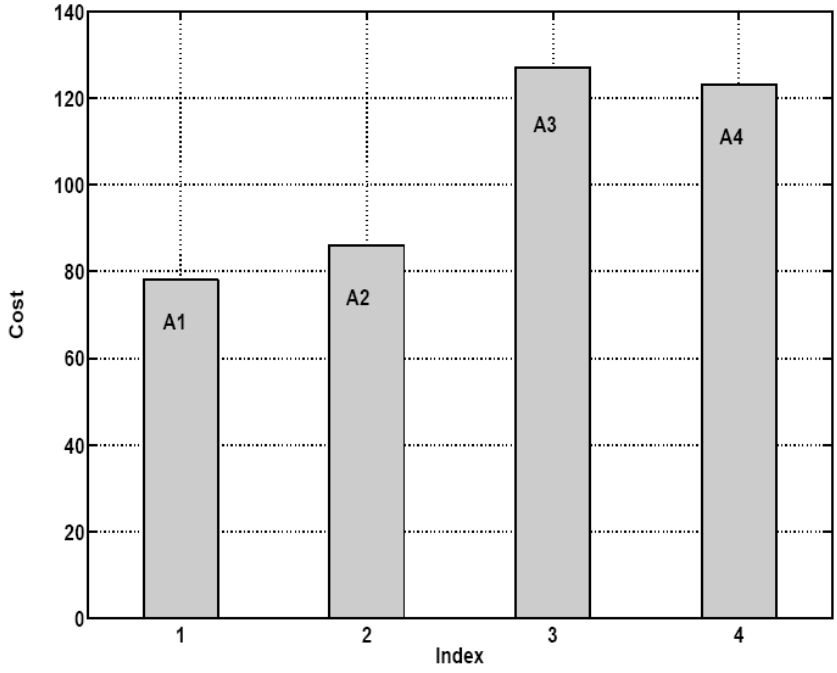

Fig. 8: Total cost of the various architectures using FCC method

4.3 Cost of the Architectures Using Wavelength Speedup Model (WSU)

In Figure 9, the cost of the various architectures are shown using WSU model. This model modifies the cost of the TWC by taking into accounts its tunable range. Here, three values of cost characterization parameter (b = 0.5, 0.7 and 0.9) are considered. For b = 0.5, the cost of the architecture A3 is highest (123 units). The following observations can be made from Figure 6,the cost of the architecture A2 and A4 are comparatively higher in comparison to architecture A1 and A3. It can also be observed that as the value of speed-up factor (b)

increases, the cost of the architectures which have larger number of TWC increases. For reasonable value of b(<0.7) the cost of the architecture A1 and A2 are comparable to each other.

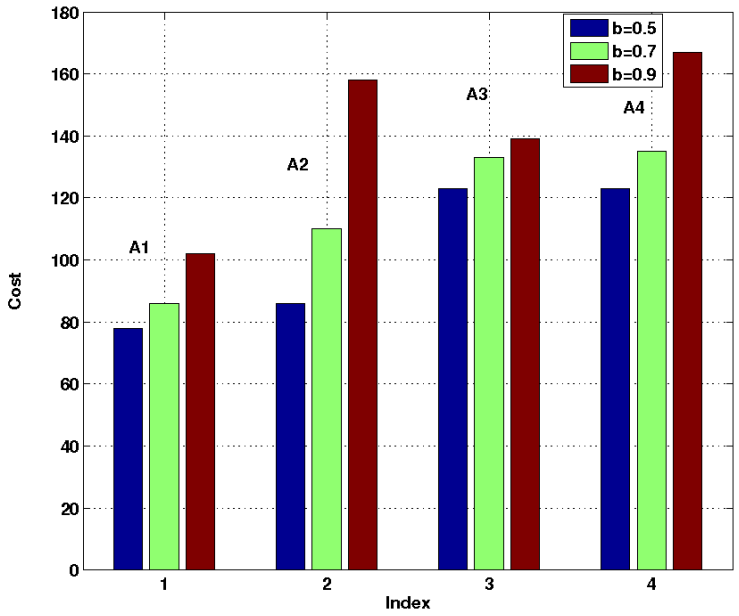

Fig. 9: Total cost of the various architectures using WSU method

V. Results and Conclusions

As we have discussed in the section 3 of the paper the complexity of the architecture A4 is highest while for architecture A2 it is lowest. Hence, the architecture A2 has inherent advantage in comparison to other architectures. The another important criterion for the switch performance is the packet loss probability. It is found from Figure 7 that the packet loss probability of the architecture A2 is lowest. In all, we are looking for a switch with lesser packet loss probability and comparatively lesser in cost. The cost vs packet loss probability curve for switch architectures using FCC model is shown in Figure 10. Under the acceptable packet loss probability i.e.$\leq 10^{-4}$ the architectures A1 and A3 are ruled out while the performance of architecture A2 is better in comparison to other architectures.

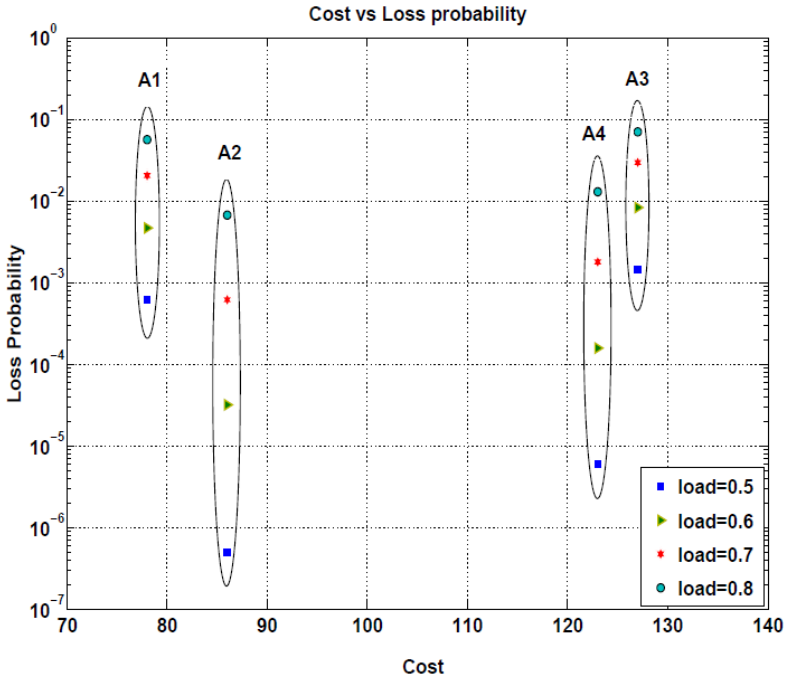

Fig 10: Cost vs. Packet loss Probability using FCC

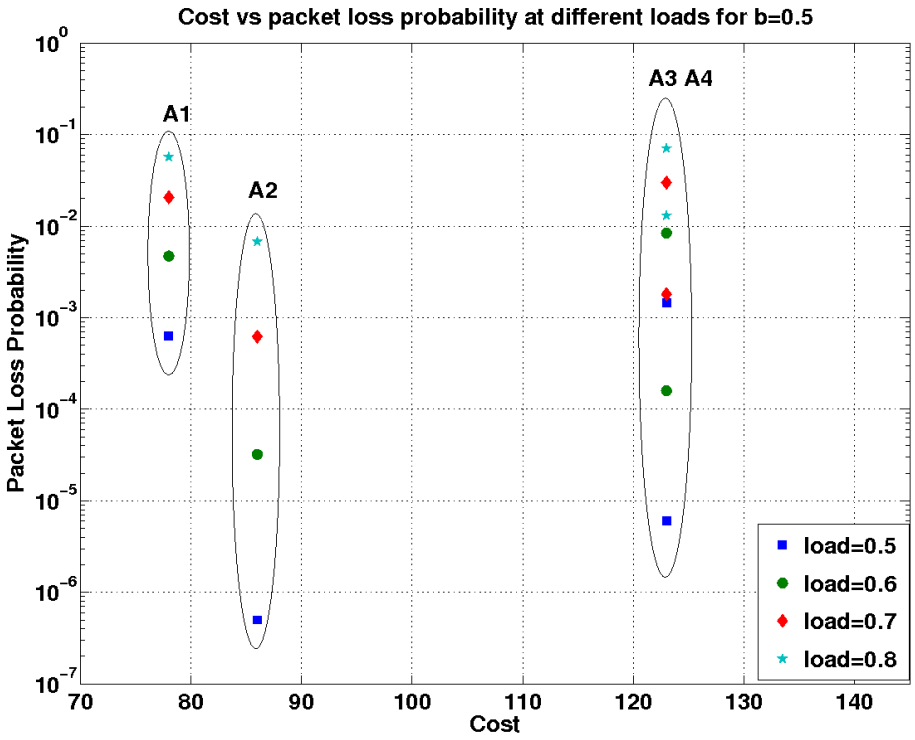

Fig. 11: Cost vs. Packet loss Probability using WSU for b=0.9

In case of the WSU model (Figure 11 - Figure13) the architectures A1 and A3 do not provide acceptable packet loss probability. However as wavelength speed-up characterization parameter (*b*) increases the cost increases but still the cost of A2 is lesser in comparison to architecture A4. Hence, it can be concluded that the architecture A2 outperform other architectures in terms of functionality, packet loss probability and optical cost.

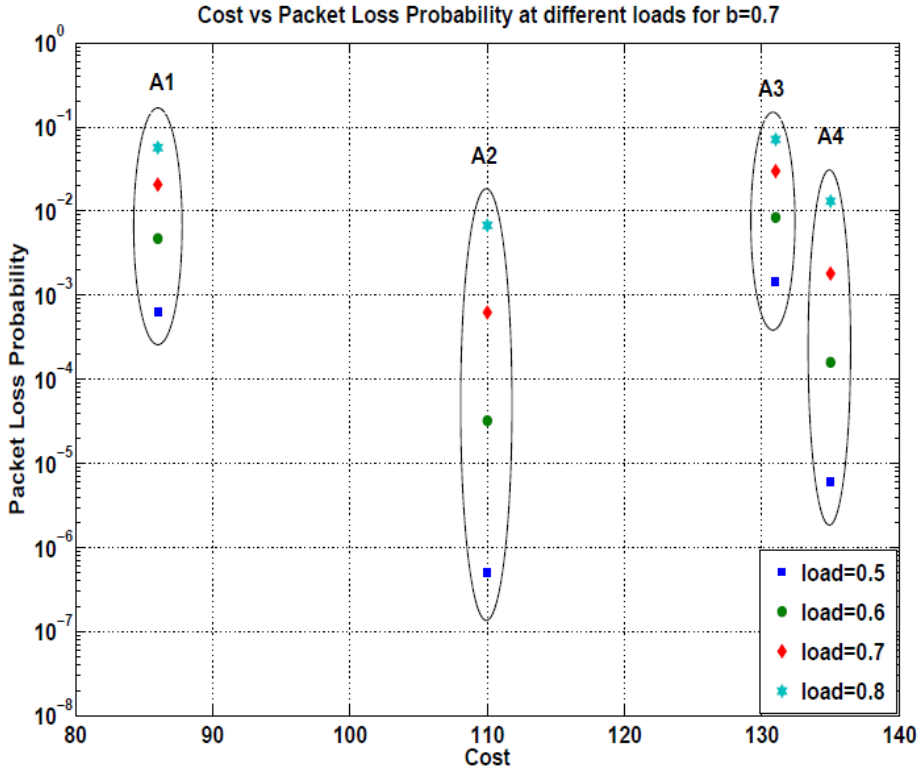

Fig 12: Cost vs. Packet loss Probability using WSU for b=0.7

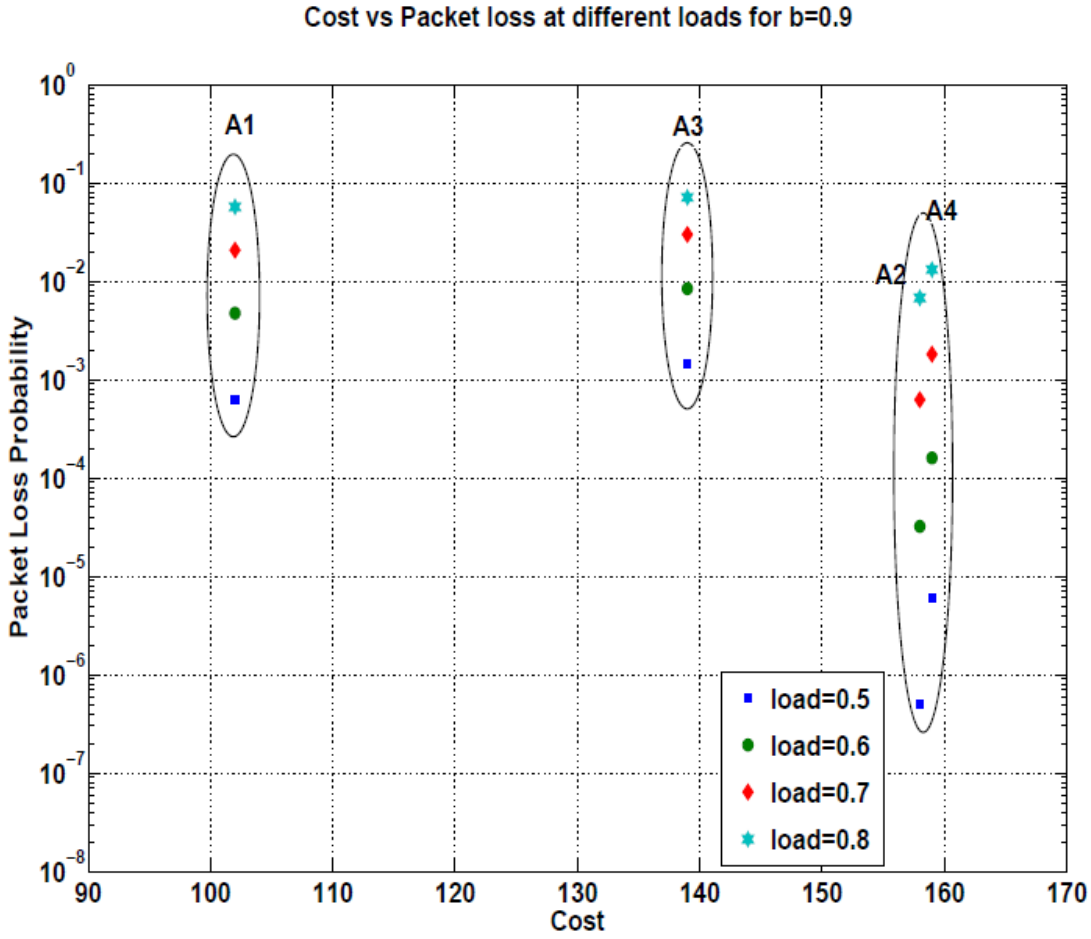

Fig. 13: Cost vs. Packet loss Probability using WSU for b=0.9

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