*I.J. Modern Education and Computer Science*, **2018, 1, 65-73**
Published Online January 2018 in MECS (http://www.mecs-press.org/)
DOI: 10.5815/ijmecs.2018.01.07

# Design and Analysis of Tunnel FET for Low Power High Performance Applications

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Received: 13 October 2017; Accepted: 29 November 2017; Published: 08 January 2018

***Abstract*—**Tunnel FET is a promising device to replace MOSFET in low power high performance applications. This paper highlights and compares the best TFET designs proposed in the literature namely: Double gate Si-based TFET, InAs TFET device and III-V semiconductor ($GaAs_{1-x}Sb_x$-InAs) based TFET device. Simulations are performed using TCAD tool and simulation results suggest that conventional DGTFET device has less on current and degraded subthreshold slope as compared to InAs and III-V semiconductor based TFET device. InAs based TFET device provides steep subthreshold slope of 61 mV/dec and off current of the order of nano-amperes at sub 1V operation thereby making it an ideal choice for low power high performance applications. The variation in the performance of the III-V HTFET device with the variation in the mole fraction is also studied in detail. Carefully choosing the mole fraction value in III-V semiconductor based HTFET device can lead to better device performance.

***Index Terms*—**TFET, Parameter variation, Subthreshold swing, Leakage power, Reliability, Band to Band tunneling, High-K dielectric material, ITRS.

## I. Introduction

Tunnel FET device is one of the promising novel devices which is giving a threat to the conventional MOSFET device to be used for low power applications. TFET device operation is based upon band to band tunneling (BTBT) mechanism and it possesses very low leakage current and steep subthreshold slope. Sub-threshold swing in case of MOSFET is ln(10) (KT/q) and at room temperature (300K), SS value is around 60 mV/dec. This fundamental challenge of reducing the SS value below 60mV/decade at room temperature can be easily overcome using a TFET device. TFET device also possess better Ion/Ioff ratio as compared to MOSFET and it is because of its low off current that TFET device is gaining confidence to be used in designing SRAMs for ultra low power applications. It is a well known fact that cache memory occupies almost 50% of the on chip area of the processor and reducing leakage in cache memory is a serious concern that needs to be addressed. A tunnel FET device possessing low off state current seems to be an immediate remedy for reducing leakage in cache memory.

A detailed description of zener tunneling and avalanche breakdown mechanism in As implanted n-p junctions had been described in detail in [1]. The main issue with a single gate TFET device is very low value of on current and poor subthreshold swing. A novel design for the double gate TFET (DGTFET) was proposed for the first time using high K dielectric material [2]. This novel device achieved SS of 57 mV/dec and an exceptionally high Ion/Ioff ratio. A novel structure of TFET device exhibiting higher on current than a conventional p-i-n TFET device was proposed in [3]. This structure was named as pocket doped TFET and has a pocket on the source side to improve the on current. Ambipolarity reduction was achieved using low doped drain extension. Modification in the TFET structure was required to be done so as to address the issue of poor on current and to achieve SS value of less than 60mV/dec. Different structures were proposed in the literature to overcome these limitations. To improve the tunneling current, low bandgap materials (eg. SiGe, Ge, InGaAs, InAs) have been widely explored for TFET prototype device design [4]. Electron Hole bilayer Tunnel FET (EHBTFET) structure had been proposed in [5] and this

 

structure exploits the asymmetric bias configuration of a DGTFET device thereby creating the two carrier layers instead of one inside the thin silicon film. The bias applied at the bottom gate is fixed and the top gate bias is used to change the electron layer concentration thereby controlling the drain current. A novel device structure called Sandwitch Tunnel Barrier FET (STBFET) had been proposed in [6]. This novel structure overcomes the issue of large voltage overshoot that occurs in conventional TFET device. Schottky Tunneling Source SOI MOSFET (STS-FET) proposed in [7] has gate controlled schottky barrier tunneling at the source and possesses high immunity to short channel effects. Analysis of the leakage current of the pocket doped TFET device shows very less change with change in temperature [8]. This signifies that pocket doped TFET device has better temperature immunity as compared to MOSFET and conventional TFET device. Vertical InGaAs/InP heterojunction TFET had been proposed in [9] for the first time. Gate overlapped source and pocket doping approach were used in [10] to improve the performance of InGaAs/InP HTFET device. The concept of leakage reduction in vertical TFET structure was proposed in [11]. This new InAs based vertical TFET device structure achieves better Ion close to ITRS requirement and SS value of less than 60 mV/dec. The discussions made till now signifies that TFETs hold promising future in the IC world and are being explored by research fraternity over the years [12,29].

The rest of the paper is organized as follows: Section II describes the TFET device structure and its operation in detail. Concept of Subthreshold swing and challenges related to TFET device are discussed in section III. Section III also highlights the models used for performing simulations on Visual TCAD tool. Related work that is reported in the literature is presented in section IV. Simulation results of different TFET devices simulated in TCAD tool are highlighted in Section V. The effect of mole fraction parameter (x) on the performance of III-V HTFET device is discussed in Section VI and finally in Section VII conclusions are drawn.

## II. TFET Device Structure and Its Operation

The basic structure of nTFET consists of a p-i-n diode with the gate region covering the entire intrinsic region. Fig.1 shows the structure of nTFET in double gate configuration with p+ source region and n+ drain region. The structure can be regarded as a gated p-i-n diode in which tunneling of electrons takes place between p+ source and intrinsic region.

In the off state the energy barrier height is high enough so that the electrons cannot tunnel through the thick depletion region which exists across p+ source and intrinsic region and hence the off current is very low. When positive voltage is applied to the n+ region and gate is also made positive with reference to the p+ source region then there occurs band bending and reduction in the energy barrier height which increases the probability of inter-band tunneling of electrons from valance band of p+ source region to the conduction band of the intrinsic region. The TFETs exhibit gate bias dependent NDR characteristics at room temperature under forward bias confirming band to band tunneling [13].

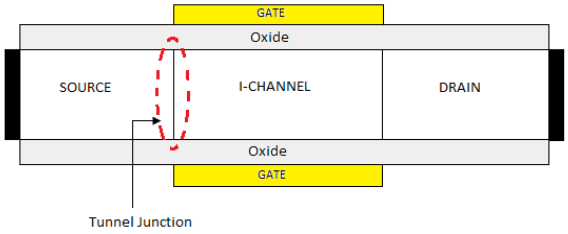


Fig.1. Basic DGTFET device structure.

Energy band diagram at different $V_{GS}$ values shows band gap narrowing effect and band bending which increases the tunneling probability across the tunnel junction. Fig.2. shows the band diagram plot of n-type DGTFET device at $V_{GS}$=0V and $V_{DS}$=1V and Fig.3 shows the band diagram plot at $V_{GS}$=1V and $V_{DS}$=1V.

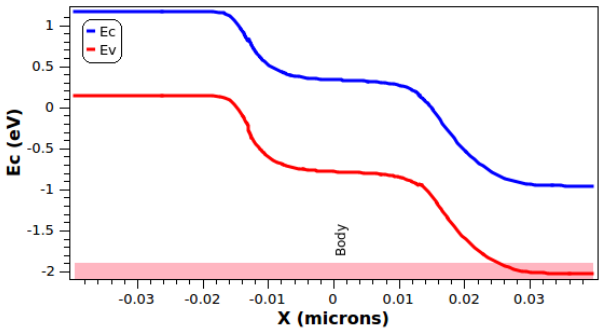


Fig.2. Band diagram of DGTFET device at $V_{GS}$=0V and $V_{DS}$=1V.

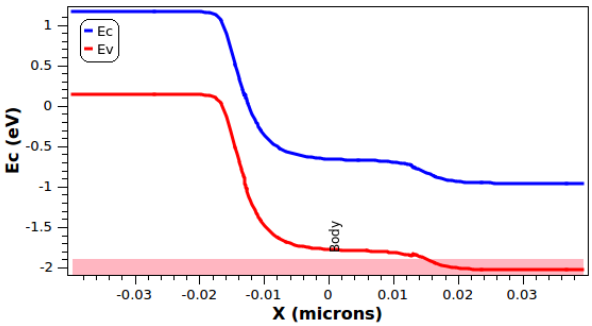


Fig.3. Band diagram of DGTFET device at $V_{GS}$=1V and $V_{DS}$=1V

Comparative band diagram is shown in Fig.4. It clearly shows that band gap reduction takes place with change in $V_{GS}$ value. A point to note is that both band bending and band gap narrowing takes place with increase in $V_{GS}$ value.

The challenge of enhancement of the on current in tunnel FET can be addressed by using a lower energy band gap material rather than silicon thereby enhancing the tunneling probability across the tunnel junction. Materials like Ge, InAs, III-V compound semiconductors

 

exhibits lower Eg value and can be used for the fabrication of TFET device. On current of the similar order can be achieved as it can be achieved using a MOSFET device. Using germanium in the source region can lead to small tunnel band gap and leads to improvement in the energy efficiency of the TFET device [14].

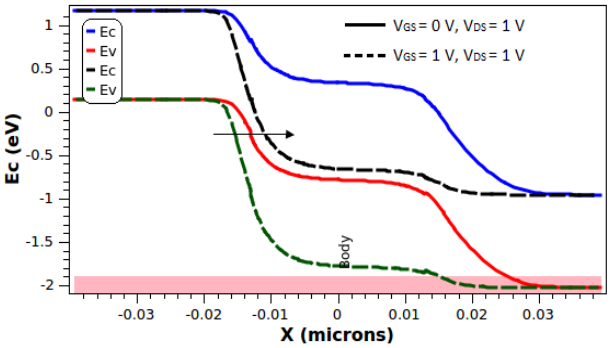


Fig.4. Comparative Band diagram of DGTFET device.

## III. Subthreshold Swing and Reliability Issues

Subthreshold swing in TFETs is defined in the same way as it is done in MOSFETs which means that it is the gate voltage which must be applied with respect to source so as to increase the drain current by one decade. A formula for calculating the subthreshold swing of TFET is proposed in [15]. This formula shows that SS of TFET is not limited to 60mV/decade. Mathematically Subthreshold Swing (SS) can be expressed as-

$$Subthreshold\ Swing = \frac{dVg}{d(\log Id)}\ mV/dec.$$

The subthreshold swing of MOSFET is limited to 60mV/dec at T=300K (room temperature) and this limitation can be overcome in TFETs which rely on interband tunneling via barrier width modulation rather than the formation of weak inversion channel between source and drain. Point sub threshold swing is the smallest value of the subthreshold swing on the ID-VG curve and on the other hand average subthreshold swing is calculated from the point where the device starts to turn on up to the threshold point (defined using constant current method [12]). The subthreshold swing in TFET is strongly dependent on the gate bias and for analyzing the switching performance it is better to consider average subthreshold swing rather than the point subthreshold swing. Literature indicates that the inherent issue of lower tunneling current that exists in silicon because of relatively higher energy band gap and lower effective tunneling mass has encouraged the designers to deploy lower band gap materials for the fabrication of TFET. Materials like Ge, InAs, GNRs, Heterojunction materials (SiGe/Si, AlGaSb/InAs, AlGaAsSb/InGaAs) etc. leads to a significant increase in the on current of TFET.

Boucart et al. [12] had proposed an analytical expression that can be used for the calculation of average sub-threshold swing of TFET device.

$$Average\ Subthreshold\ Swing = \frac{Vth - Voff}{\log\left(\frac{Ith}{Ioff}\right)}$$

where *Voff* is the gate source voltage at which drain current is minimum (*Ioff*), *Vth* is the threshold voltage at the threshold point (point at which Ids is $10^{-7}$ A/um). A practical expression for calculating the effective sub threshold swing of TFET device was proposed in [16]. According to this new practical definition:

$$Vth = \frac{Vdd}{2} \text{ and } Ith = Ids(Vgs=Vdd/2)$$
$$Voff = 0 \text{ and } Ioff = Ids\ (Vgs=0)$$

Hence Subthreshold Swing expression can be rewritten as-

$$SS = Vdd/[2\log(Ith/Ioff)].$$

SS value decreases as *Vgs* value decreases. *Vgs* directly controls the tunnel junction bias (band overlap). Gate is placed to align the field with the internal field at the tunnel junction. Gate field adds to the internal field and increases the tunneling probability.

Cogenda Visual TCAD is used for performing device simulations. Kane's Local BTBT model is used along with SRH model for device simulation. For mobility Lombardi model is used in this work. A method to calculate the parameters A and B of Kane's direct and indirect tunneling models at different tunneling directions for Si, Ge and $Si_{1-x}Ge_x$ was discussed in [17]. The calculation of band-to-band generation rate in uniform electric field reveals that direct tunneling always dominates over indirect tunneling in Ge [17].

*Kane's Band to Band Tunneling Model:*

Kane's tunneling model is used in the simulator to calculate the carrier generation by band to band tunneling phenomenon. The carrier generation rate is calculated using the following expression derived from [17].

$$G^{BB} = A.BTBT.\frac{E^2}{\sqrt{E_G}}.\exp\left(-B.BTBT.\frac{E_G^{3/2}}{E}\right)$$

where Eg is the energy band gap of the material, E is the magnitude of electric field, A.BTBT & B. BTBT are empirical fitting parameters which can be defined in the simulation by the user. Values of these two parameters are tuned to match with the experimental Id-Vgs characteristics.

*Challenges in TFET:*

 

Unlike CMOS, TFETs exhibit unidirectional conduction due to their asymmetric source-drain architecture [18,31]. TFET operates at low supply voltage range ($V_{dd}$ < 0.5V) to outperform CMOS, reliability issues can have profound impact on the circuit design from practical application perspective [19]. Subthreshold swing of TFET is found to be more robust against PBTI as compared with MOSFETs [20]. Charges present in the Si-Oxide interface and Oxide-Oxide interface affects the performance of the TFET device. Tunnel FETs also show relatively less variation to fixed interface charges and can replace MOSFETs in circuits to combat against NBTI and PBTI effects [21]. Investigation of p-n-i-n TFET device carried out in [22] reveals that TFET structure has improved reliability as compared to conventional TFET structure. Reduced interface trap generation and gate leakage is seen in p-n-i-n TFET along with less variation in the threshold voltage with change in the oxide thickness and Si film thickness. The gate dielectric plays an important role in enhancing the performance of a p-n-p-n TFET device. In p-n-p-n TFET device use of high gate dielectric constant is preferable for enhancing the gate control over the channel, while a low fringe dielectric constant is useful to increase band to band tunneling probability [23]. Use of spacer in TFET device leads to suppression in the ambipolar conduction [24]. Overlapping the gate on the drain can also suppress the ambipolar conduction, which is an inherent property of a TFET device [25]. Doping Less Tunnel FET device is expected to be free from random dopant fluctuation [26] and this configuration also possesses similar performance as that of the corresponding doped TFET device. Use of TFET device in low power high performance application circuits like SRAM can lead to several advantages like improvement in the noise margins, power reduction and reliability. Different SRAM cell topologies are proposed in [12,19,27] have shown tremendous performance under ultra low supply voltage and thereby showing the possibility of designing complete TFET based SRAM. DGTFET-based dynamic memory at sub-100-nm regime has been discussed in detail in [30] with main emphasis on device optimization by tuning the misalignment, lateral spacing between the gates (*L*gap*)* and an underlap (*L*un*)* between the back gate and drain region.

## IV. Related Work

Literature review suggests that the on current of tunnel FET can be improved by making use of lower band gap semiconductor material rather than silicon for the fabrication of tunnel FET. Datta et al.[19] have made use of $GaAS_{0.1}Sb_{0.9}$ material for the fabrication of source region and InAs material for the fabrication of channel and drain regions respectively. This proposed III-V semiconductor based TFET device was able to achieve 7 times improvement in Ion as compared to the Si based FINFET device of similar dimensions. Si DGTFET device proposed in [2] achieved on current of the order of 0.23 mA/μm with an average subthreshold slope value of 57 mV/dec. It was the first Si based DGTFET device which was able to achieve excellent performance parameters. Ambipolar conduction is an important issue related to tunnel FETs. Costin Anghel et al.[24] proposed a Si based TFET device that suppressed the ambipolar current to as low as $10^{-14}$ μA/μm by making use of low-K spacer in the LSHG structure along with the introduction of under lapping between gate and drain region. The challenge of fabricating the III-V compound semiconductor was addressed in [28]. Waho et al.[28] demonstrated that $GaAs_{1-x}Sb_x$ homogeneous epitaxial layers can be grown on GaAs substrate over a wide range of mole fraction x($0.3<x<0.9$).

The proposed work optimizes the performance of III-V semiconductor based heterojunction TFET device by tuning the mole fraction parameter (x) in $GaAs_{1-x}Sb_x$ semiconductor material. For comparative analysis two other TFET device structures have been designed using Si and InAs semiconductor material.

## V. Resuts and Discussions

In this work three different designs of TFET are analyzed namely: Si based double gate TFET, InAs based TFET, $GaAs_{1-x}As_x$-InAS based TFET device. The various device parameters used in the simulation are highlighted in Table I.

Table I. Parameter Table For Ntfet

| Parameter | Value for Si double gate nTFET | Value for InAs double gate nTFET | Value for III-V heterojunction nTFET device |
|---|---|---|---|
| Gate Length Lg in (nm) | 30 | 20 | 40 |
| Source Doping Concentration P-type (Ns) | 1e+20 | 4e+19 | 4e+19 |
| Drain Doping Concentration N-type (Nd) | 5e+18 | 6e+17 | 5e+17 |
| Channel Doping Concentration (Nch) | 1e+16 | 1e+16 | 1e+15 |
| Physical oxide thickness Tox in (nm) | 2.5 | 1 | 13.5 |
| Si body thickness, Tsi in (nm) | 7 | 5 | 5 |
| Dielectric constant of the material under consideration (Kdielectric) | 21 | 21 | 21 |
| Gate source overlap in (nm) | 2 | 2 | 2 |
| Work function of the gate material in (eV) | 4.2 | 4.88 | 4.45 |

 

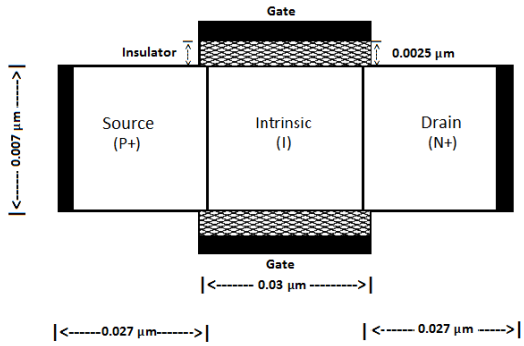


Fig.5. Schematic diagram of Si-DGTFET device.

The schematic diagram and transfer characteristics of Si based double gate nTFET device are shown in Fig.5 and Fig.6 respectively. The off state current in this configuration is extremely low around $9.43x10^{-17}$ A/µm (calculated at VGS = 0V). This device suffers from poor on current and low average subthreshold swing. On current value of 0.00252 mA/µm (calculated at VGS = 1.5 V) and average subthreshold swing of 116.2 mV/dec is achieved in this device configuration, Vds is kept at 1.0V. Low value of the on current and reduced subthreshold swing are limiting factors for this device to be deployed in applications like SRAM design which needs high speed of operation.

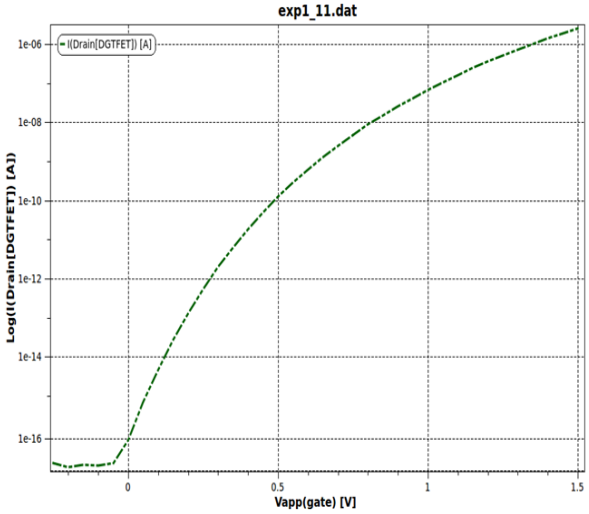


Fig.6. Id-Vg curve of double gate nTFET device simulated in Visual TCAD.

On current boosting can be achieved by using low energy band gap material instead of silicon for TFET device fabrication. Low energy band gap material like InAs will increase the tunneling probability across the tunnel junction and hence will result in improvement in the on current and subthreshold swing of the TFET device. Fig.7 shows the schematic diagram double gate InAs based nTFET device designed in TCAD. DC characteristics of InAs homojunction nTFET device is shown in Fig.8.

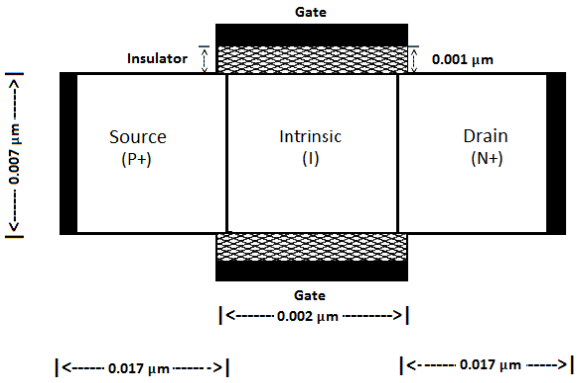


Fig.7. Schematic diagram of InAs homojunction nTFET device simulated using TCAD tool.

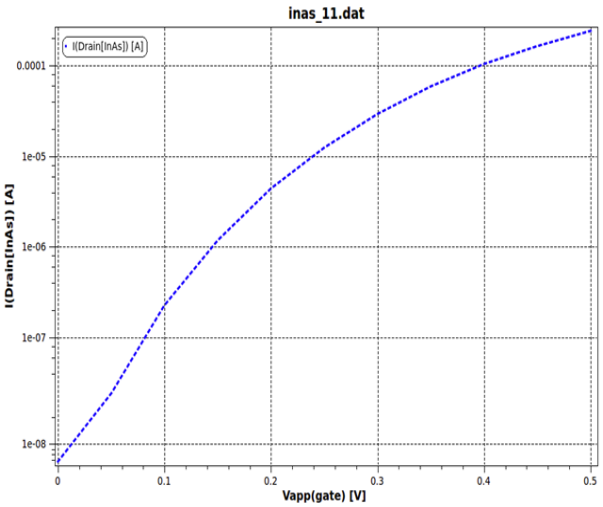


Fig.8. Id-Vg curve of InAs homojunction nTFET device.

It is clear from Fig.8 that low value of the off current of the order of 3.39 nA/µm (calculated at VGS = 0V) and high value of on current 0.24 mA/µm (calculated at VGS = 0.5V) is achieved in this device configuration, Vds in this case is kept at 0.5V. The prime reason for the improvement in the on current is the low energy band gap of InAs material (0.45 eV) which is very small in comparison to silicon (1.1 eV). Improved average subthreshold swing value of 61.2mV/dec shows a significant improvement as compared to conventional Si based DGTFET device. This device configuration has promising performance parameters thereby making it an ideal candidate for low power high performance applications. The off current in InAs based TFET device is higher than the conventional Si based TFET device but still it is low enough for making it a suitable choice for low power VLSI circuit design. Literature review suggests that on current of the order of MOSFET can be achieved by designing TFET device using III-V compound semiconductor material. Datta et al. [19] proposed a heterojunction TFET (HTFET) device made using III-V semiconductor material ($GaAs_{1-x}Sb_x$-InAs)

 

and similar design is analyzed in this work but with a different value of the mole fraction parameter. The device proposed in [19] has a very high value of the off current which is the major challenge to be addressed so as to make sure that III-V semiconductor based TFET device can be deployed in low power applications. Fig.9. shows the schematic diagram of HTFET device and Id-Vg curve of this device are shown in Fig.10. The on current value of 0.0201 mA/μm (calculated at VGS = 0.7 V) and improved subthreshold swing of 95.64 mV/dec is achieved in the simulated III-V semiconductor material based HTFET device using mole fraction value of 0.625. Off current in this new structure is significantly reduced and is of the order of 0.196nA/μm. It is found that mole fraction x is an important parameter which has to be calibrated so as to improve the device performance in terms of the off current. Application circuits like SRAM will remain in the off state for most of the time and in case the off current is high then it will lead to considerable increase in the standby power consumption. On current and average subthreshold swing in the simulated device (Fig.9) is less as compared to the simulated InAs based double gate TFET device. The combined Id-Vg plot of all the three simulated devices presented in this work is shown in Fig.11. It clearly shows the better performance of InAs based TFET device which outperforms the other two devices in terms of on current and subthreshold swing and also possess low off current. Ion/Ioff ratio of the conventional Si based DGTFET device is maximum out of the three configurations but it is purely due to the extremely low value of the off current in the Si based DGTFET device. For high performance application circuits like SRAM both on current and off current are equally important and thus improvement in the on current is very much needed so as to deploy TFET device in designing SRAM cell.

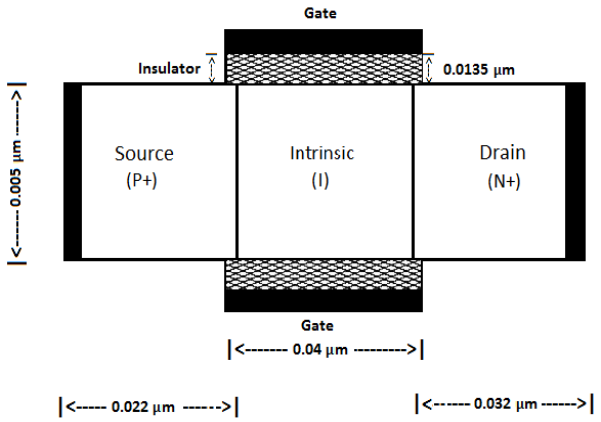


Fig.9. Schematic diagram of HTFET device.

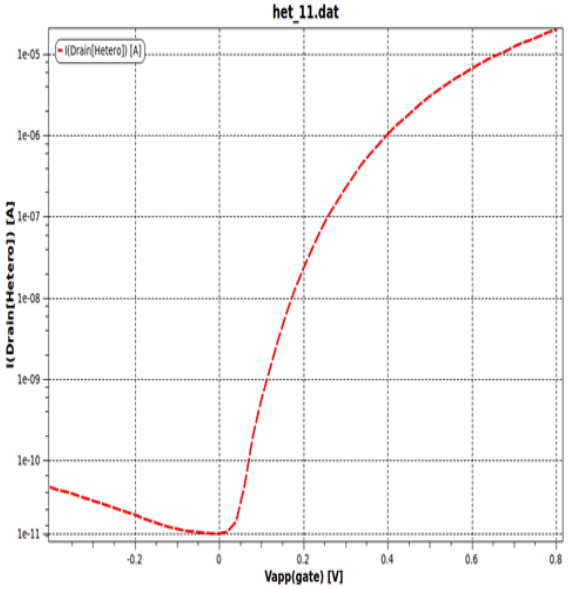


Fig.10. Id-Vg curve of III-V semiconductor based nTFET device.

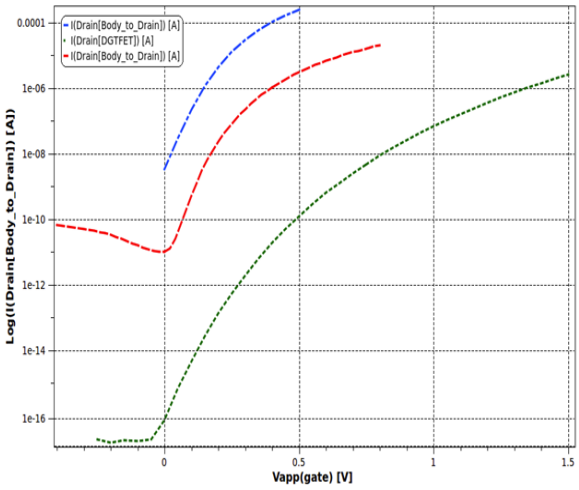


Fig.11. Combined curve for all three TFET configurations.

Table II highlights all the performance parameters calculated for the three TFET devices simulated using TCAD tool.

Table II. Performance Parameters

| Tunnel FET device | Device Performance Parameters | | | |
|---|---|---|---|---|
| | Sub threshold swing (SS) in mV/dec | On current (Ion) in mA/um | Off current (Ioff) in nA/um | Ion to Ioff ratio |
| Double gate Si TFET | 116.3 | 0.00252 | $9.43x10^{-8}$ | $10^{11}$ |
| Hetero junction double gate TFET | 95.64 | 0.0201 | 0.196 | $1.53x 10^{4}$ |
| InAs based double gate TFET | 61.2 | 0.24 | 3.39 | $7.13x 10^{4}$ |

 

It can be seen from Table II that the performance of InAs based TFET device is better in terms of on current and subthreshold slope. SS value of 61 mV/dec shows that this device has potential to perform in high performance VLSI circuits. It also has good Ion/Ioff ratio. SS value is minimum in case of conventional Si based DGTFET device but this topology possesses very low leakage current value and this is the main reason why this device topology has the best Ion/Ioff ratio as compared to other TFET topologies. HTFET device based on III-V semiconductor device possess steep SS value of 95.64 mV/dec and better on current as compared to conventional Si based DGTFET device but this device configuration has performance characteristics which are strongly dependent on mole fraction of antimony (x).

## VI. Mole Fraction Variation Analysis

The performance of $GaAs_{1-x}Sb_x$ – InAs based TFET device is affected by mole fraction parameter (x). Fig.12 shows the Id-Vg curve of the HTFET device designed using III-V semiconductor material under different values of antimony concentration.

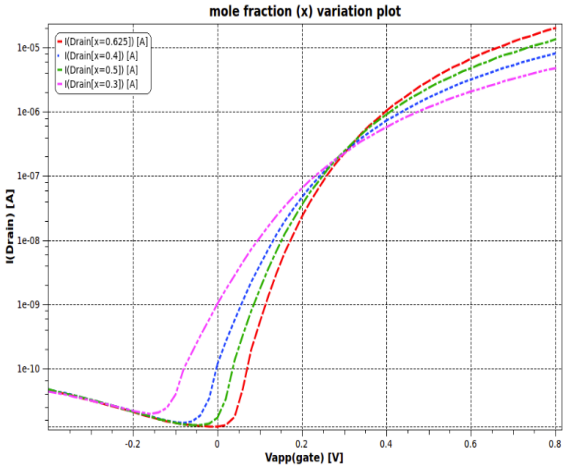


Fig.12. Mole fraction variation analysis curve.

Results published in [28] indicate that over a wide range of mole fraction $0.3<x<0.9$ $GaAs_{1-x}Sb_x$ homogeneous epitaxial layers can be grown on GaAs (001) substrate. The device optimization has been performed by varying the x values from 0.3 to 0.625. It is clear from Fig.11 that on current of the device increases with increase in the concentration of antimony in $GaAs_{1-x}Sb_x$ compound semiconductor. The prime reason for increase in the on current with increase in the mole fraction value is the reduction in the tunnel width due to reduction in the band gap energy with increase in gate to source voltage. The probability of tunneling will increase with reduced barrier width which ultimately will lead to increase in the on current of the device. The increase in the $V_{GS}$ value will increase the electric field across the tunnel junction and the energy band gap modulation will take place. The effect of band gap reduction and narrowing is more at higher value of mole fraction. It is important to also see the off current variation with change in the mole fraction x. It is seen that off current value is less at x=0.625 as compared to its value at x=0.3. The prime reason for this phenomenon is that the number of available states in the conduction band is less in the off state which leads to lower tunneling across the tunneling junction at lower gate voltage.

## VII. Conclusion

This paper investigated three different TFET designs namely: Si-based DGTFET, InAs based TFET and $GaAs_{1-x}Sb_x$–InAs HTFET device. Simulation results show that mole fraction (x) is an important parameter for optimizing the performance of HTFET device. At x value of 0.625, HTFET device achieves optimal performance in terms of subthreshold slope, on current and off current. InAs material has lower energy band gap value and TFET device designed using InAs material is able to achieve best subthreshold slope of 61.2mV/dec and highest on current of 0.24 mA/μm as compared to other two TFET device configurations that are investigated in this work. Use of low energy band gap material like InAs and III-V semiconductor material in TFET device fabrication can lead to achievement of SS value of below 60 mV/dec and on current similar to that of a MOSFET. Tunnel FET device has shown tremendous promise of becoming a potential candidate for replacing MOSFET in low power high performance applications. The journey of advancement of TFET device has lead to several breakthroughs but still there are lot many challenges that need to be overcome which includes: Accurate gate alignment, low resistance contacts, abrupt and accurate tunnel junctions, gate stacks with low interface trap density and advanced processes for nanoscale III-V semiconductor based transistors.

## Acknowledgment

The authors would like to thank the management of Manav Rachna Educational Institutions for providing the research facilities for carrying out this work.

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**How to cite this paper:** Umesh Dutta, M.K.Soni, Manisha Pattanaik, "Design and Analysis of Tunnel FET for Low Power High Performance Applications", International Journal of Modern Education and Computer Science(IJMECS), Vol.10, No.1, pp. 65-73, 2018.DOI: 10.5815/ijmecs.2018.01.07

 