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A Novel Quaternary Full Adder Cell Based on Nanotechnology

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Abstract—Binary logic circuits are limited by the requirement of interconnections. A feasible solution is to transmit more information over a signal line and utilizing multiple-valued logic (MVL). This paper presents a novel high performance quaternary full adder cell based on carbon nanotube field effect transistor (CNTFET). The proposed Quaternary full adder is designed in multiple valued voltage mode. CNTFET is a promising candidate for replacing MOSFET with some useful properties, such as the capability of having the desired threshold voltage by regulating the diameters of the nanotubes, which make them very appropriate for voltage mode multiple threshold circuits design. The proposed circuit is examined, using Synopsys HSPICE with the standard 32 nm CNTFET technology with different temperatures and supply voltages.

Index Terms—Carbon nanotube FET (CNTFET), Quaternary logic, Full Adder, Multiple-Vth design, Nanoelectronics.

I. Introduction

Traditional computer systems use binary logic for their operations. However, Multiple-valued logic (MVL) circuits have been designed over the last decades as an alternative to binary circuits. The main advantage of the MVL is reduction in the number of interconnections, which is a serious problem in binary integrated circuits of the present time.

Multiple-valued logic seeks to improve the information processing efficiency of a circuit by transmitting more information on each signal line than the simple binary logic and by implementing complex functions of the inputs in a single gate. However, MVL using has been restricted due to the fact that compact and stable MVL circuits are hard to be designed, the noise margins on multiple valued lines are reduced and most importantly there is a need to perform conversions to and from the binary world. Accordingly, designers using the MVL paradigm have mostly focused on the ternary (i.e. radix 3) and the quaternary (i.e. radix-4) number systems. Ternary system consists of three digits, namely {0, 1, 2} and quaternary system consists of four digits {0, 1, 2, 3}. However, quaternary logic seems to be more interesting due to the simple conversion between quaternary signals and binary signals.

On the other hand, scaling down the feature size of the metal-oxide semiconductor (MOS) technology deeper in nano-ranges leads to numerous critical challenges and problems, which will considerably reduce its suitability for energy efficient applications in the time to come. To overcome these problems, such as short channel effects, reduced gate control and high leakage power dissipation, researchers are working towards new technologies. These technologies, such as single electron transistor, quantum dot cellular automata and carbon nanotube field effect transistor (CNTFET) are being studied to replace the customary silicon based CMOS technology in the near future [1]-[3]. Among these emerging nanotechnologies, CNTFET seems to be more appropriate on account of its likeness with MOSFET in terms of inherent electrical properties which makes it possible to utilize previously designed CMOS structures in the CNTFET technology without any significant modifications. Moreover, the unique one-dimensional band structure of the CNTFET represses backscattering and causes near-ballistic operation, which results in very high-speed operation [4].

One of the important properties of CNTFETs which is very useful for transistor sizing of complex circuits is the same mobility for N-FET and P-FET and consequently same current drive capability. Generally CNTFETs are faster than MOSFETs and also consume less power.

MVL circuits can be designed either in current mode or voltage mode. CMOS voltage mode MVL circuits are based on multiple-threshold design which can be achieved by applying different bias voltages to the bulk terminal of transistors. This method is not efficient and leads to very complex and high-cost fabrication. In a

CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT. Since, a multiple threshold design can be carried out by adopting CNTs with different diameters for different CNTFETs.

Accordingly, proposing new efficient CNFET-based designs for quaternary logic is of an interest. In this paper we proposed an efficient quaternary full adder cell based on carbon nanotube field effect transistor. Full adder cell is one of the most important ingredients in a processing system and designing a high-performance Full adder cell would increase the performance of whole system [5].

The organization of the rest of the paper is as follows: section 2 reviews the carbon nanotube field effect transistor. The proposed CNFET-based quaternary Full adder is described in section 3. In section 4 the simulation results are presented and finally the paper is concluded in section 5.

II. Carbon Nanotube Field Effect Transistors (CNFETs)

Carbon nanotube is fundamentally considered as a sheet of graphite rolled into a tube with a diameter of a few nano meters and length of up to several micro meters. CNTs are classified into single-walled CNTs (SWCNTs), made up of a single cylinder, and multi-walled CNTs (MWCNTs), made up of more than one cylinder [6]. The way the graphite sheet is rolled is represented by a pair of indices called chiral numbers. These indices indicate the conductivity of a CNT. A CNT with $n\text{-}m=3k$ ($k \in Z$) is metallic; otherwise it is a semiconductor which can be used as the channel of a CNFET.

CNT is the most promising candidate for creating transistors on a scale smaller than silicon transistors due to its outstanding electrical properties, such as quasi-ballistic carrier transport and suppression of short-channel effects due to one-dimensional electron transport. Furthermore, a CNTFET has similar I-V characteristics with a well-tempered MOSFET but with a considerably smaller channel-length modulation parameter [7].

Fig. 1 shows a typical CNTFET device. The distance between the centers of two adjacent CNTs below the same gate of a CNTFET is called Pitch, which has a direct impact on the width of the contacts and the gate of the transistor.

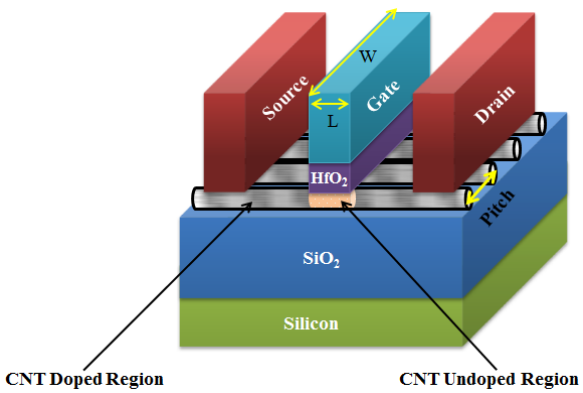

Fig 1. MOSFET-like CNTFET Device

The width of the gate of a CNTFET can be calculated based on the following equation [8]:

$$W_{gate} = Max(W_{Min}, (N-1)Pitch + D_{CNT}) \quad (1)$$

Where, W_{min} is the minimum gate width and N is the number of tubes underneath the gate. CNTFETs ease circuit designing and increase circuit's performance as the threshold voltage of a CNTFET is proportional to the inverse of the diameter of its nanotube. The threshold voltage of a CNFET is calculated as:

$$V_{TH} = \frac{0.436}{D_{CNT}(nm)} \quad (2)$$

$$D_{CNT} = \frac{a\sqrt{n^2 + m^2 + nm}}{\pi} \quad (3)$$

This feature of CNTFETs indicates that by changing the CNTFETs diameters can easily acquire different transistors with different turn on voltages.

This practical characteristic makes CNTFET very appropriate for designing voltage-mode MVL circuits. Where, a(≈0.249 nm) is the carbon to carbon atom distance, Vπ (≈3.033 eV) is the carbon π–π bond energy in the tight bonding model and DCNT is the diameter of the nanotubes.

Different types of CNTFETs have been presented so far [9]. One of them is Schottky Barrier CNTEF (SB-CNTFET). SB-CNTFET has direct contact between the semiconducting CNT and the metal; hence Schottky Barrier exists at the metal nanotube junction. In this type of CNTFETs by changing the barrier height at the metal semiconductor interface, gate modulates the injection of carriers in the nanotube. Due to exhibition of strong ambipolar characteristics, SB-CNTFETs are not suitable for using in CMOS logic families. Another type of CNTFETs is MOSFET-like CNTFET (MOS-CNTFET) which exhibit unipolar behavior unlike SB-CNTFET. In this MOSFET like device, the ungated portions (source and drain regions) are heavily doped and the CNTFET operates on the principle of barrier height modulation by application of the gate potential. The conductivity of MOS-CNTFET is modulated by the gate-source bias. Both SB-CNFETs and MOS-CNFETs are used for high speed design because of their high ON current. However, the other type of CNTFET, band-to-band tunneling CNTFET (T-CNTFET) is utilized for ultra-low-power design on account of its low ON current and supper cut-off attributes.

III. Proposed Quaternary Full Adder Cell

Quaternary logic includes four significant logic levels which can be demonstrated by "0", "1", "2" and "3" symbols. These logic levels are commonly equivalent to 0 V, $1/3V_{DD}$, $2/3V_{DD}$ and V_{DD} voltage levels, respectively.

In this work, we propose a new quaternary full adder cell based on Carbon nanotube field effect transistors.

Quaternary full adder has three inputs (A, B, C) and two outputs (Sum, Cout) which can take values of 0,1,2,3. Sum and Cout can be defined based on equations 3 and 4.

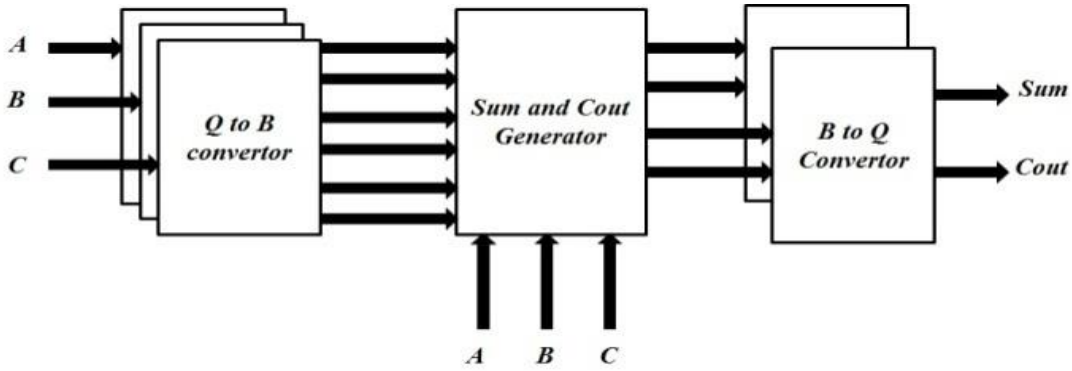

Fig 2. The proposed quaternary full adder (CQFA)

$$Sum = \begin{cases} A+B+C & if \;\; A+B+C<4 \\ A+B+C-4 & if \;\; 4\le A+B+C<8 \\ A+B+C-8 & if \;\; A+B+C\ge 8 \end{cases} \quad (4)$$

$$Cout = \begin{cases} 0 & if \;\; A+B+C<4 \\ 1 & if \;\; 4\le A+B+C<8 \\ 2 & if \;\; A+B+C\ge 8 \end{cases} \quad (5)$$

Although the concept of multiple valued logic has existed for a long time, but there are rare efforts on designing quaternary full adder. Nearly all quaternary full adder circuits which have been proposed so far have been designed based on multiple supply voltage and assumed that *carry in* is 0 or 1 [10]-[12], which is an unrealistic simplification. However, in this paper we propose a quaternary full adder which has a single supply voltage and assume that *carry in* can take all four possible values (0, 1, 2, 3).

The proposed quaternary full adder is constructed of three distinct modules including quaternary to binary converter, sum/carry generator and binary to quaternary converter respectively. At the first step a quaternary value is given to the quaternary to binary converter in order to create input binary values. Afterwards, sum and carry are calculated based on the binary and quaternary values and finally the outputs of sum and carry generators are fed to a binary to quaternary converter which gives quaternary output signals. Fig 2 shows how these three modules connect to each other. In the next subsections, each of these modules is described precisely.

A. Quaternary to Binary Converter

The proposed quaternary to binary converter circuit consists of three binary inverters with different thresholds, two binary NANDs and a binary exclusive-NOR (XNOR) gate. In the proposed Q to B converter the transition point of the binary inverters are specified by setting proper threshold voltage for their CNTFETs, which are determined by the diameter of their CNTs according to equation 2. In this design, for CNTFETs with diameters of 2.27 nm, 1.487 nm and 0.783 nm, the chirality numbers would be (29, 0), (19, 0) and (10, 0) and consequently, the threshold voltage values (|Vth|) would be 0.192 V, 0.293 V and 0.557 V, respectively. According to Fig 3, the operation of the proposed Q to B design can be briefly described as follows: when the input value is 0 V the output of all inverters are V_{DD}. so *out*1 and *out*0 will be 0V. When the input value reaches around 1/3 V_{DD} the output of the first inverter is 0 and two others are V_{DD}, consequently *out*1 and *out*0 will be 0 and V_{DD} respectively. Moreover if the input value is around 2/3 V_{DD} the output of two first inverters are 0 and the last one is V_{DD}, therefore *out*1 and *out*0 are V_{DD} and 0 respectively. Finally if the input value is V_{DD} outputs of all inverters are 0, therefore *out*1 and *out*0 are V_{DD}.

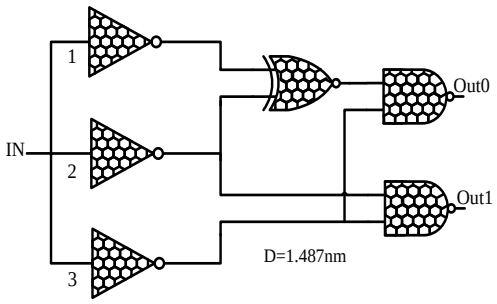

Fig 3. Quaternary to Binary converter

B. Sum and Carry generator

After generating the binary values of all three quaternary inputs, Sum and Cout can be calculated based on binary logic. Therefore, in this step of the design Sum0, Sum1, Cout0 and Cout1 are produced according to the values shown in Table 1. Sum0 has a simple function based on equation 6.

$$Sum0 = A0 \oplus B0 \oplus C0 \quad (6)$$

We used ordinary binary XOR for designing Sum0. However, producing Sum1 and Cout1 by this method is

not efficient at all and leads to a large number of logic gates and consequently a very large number of transistors. Therefore it is necessary to find a more efficient approach for generating the Sum1 and Cout1signals. A novel efficient design for creating Cout0, Cout1and Sum1 is proposed in this section of the paper, based on capacitive voltage division of three quaternary inputs and using CNTFET-based inverters with different thresholds.

According to Table 1, when the sum of inputs is 4, 5, 6 or 7, Cout0 is V_{DD}, and when the summation of inputs is 8 or 9, Cout1 is V_{DD}. In order to have the sum of the three inputs, three input capacitors are utilized. These three capacitors give us the scaled summation of inputs by voltage division and produce a value between 0 V to $_{VDD}$. Capacitors can be implemented by CNTFET. One plate of CNTFET capacitor is the gate and the other plate is the source-drain-substrate junction (Fig 4). The capacitance of CNTFET capacitor is proportional to the number of CNTs under the gate and can be computed as follows [7]:

$$C_{CNFET} = NC_{CNT} + C_{gate} \quad (7)$$

Where N is the number of CNTs, CCNT is the capacitance of one CNT in the CNTFET device and Cgate is the gate size capacitance of the CNTFET.

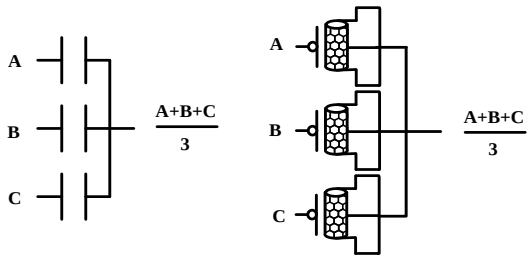

Fig 4. Input summation by CNTFET capacitors

As it is shown in Fig 5 by utilizing two inverters with logical thresholds of 3.5 and 7.5 we can generate Cout0 and Cout1. When the sum of inputs is between 4 and 7 the outputs of the first and the second inverters are 0 and V_{DD} respectively.

Consequently, the output of the third and the forth inverters are V_{DD} and 0, respectively. By these values, pCNTFET is ON and nCNTFET is OFF and consequently Cout0 is V_{DD} and Cout1 is 0. Moreover if the sum of inputs is 8 or 9 the output of both first and second inverters are 0. So the output value of the third and fourth inverters is V_{DD}. Consequently PCNTFET is OFF and NCNTFET is ON. Therefore Cout0 and Cout1 would be 0 and V_{DD} respectively.

Figure 6, illustrates proposed circuit for producing Sum1. According to Table 1, Sum1 is V_{DD} when the sum of inputs is 2, 3, 6 and 7. For the summation of the input values, three input capacitors are used similar to previous proposed circuit. In this circuit inverters with different thresholds are used in order to tune transition regions. When the sum of the inputs is 2 and 3 output of the first inverter is 0 and output of other three input inverters is V_{DD}. As a result, the output of inverter 5 is V_{DD} and the output of 6, 7 and 8 inverters is 0. Therefore T1 is ON and consequently Sum1 would be V_{DD}.

Table 1. Truth table of Quaternary Full adder

$\sum in$	Sum1	Sum0	Cout1	Cout0
0	0	0	0	0
1	0	1	0	0
2	1	0	0	0
3	1	1	0	0
4	0	0	0	1
5	0	1	0	1
6	1	0	0	1
7	1	1	0	1
8	0	0	1	0
9	0	1	1	0

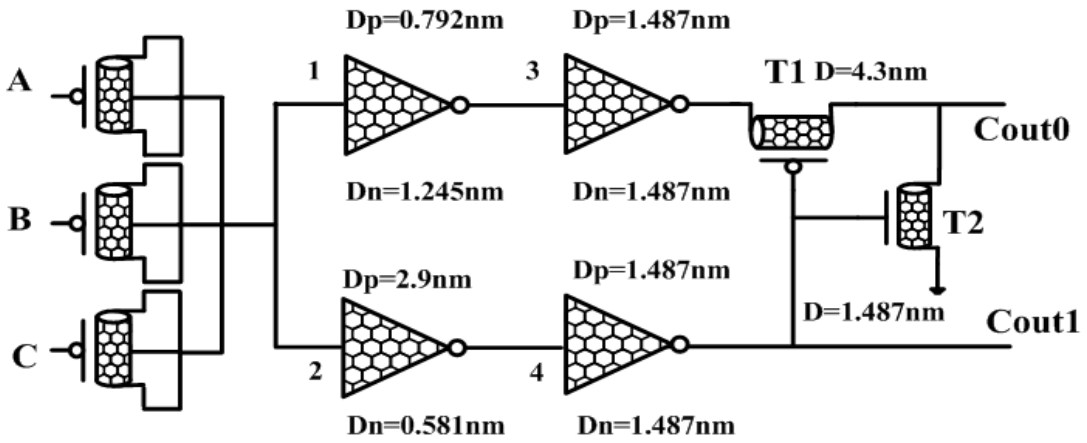

Fig 5. Cout0 and Cout1 generator

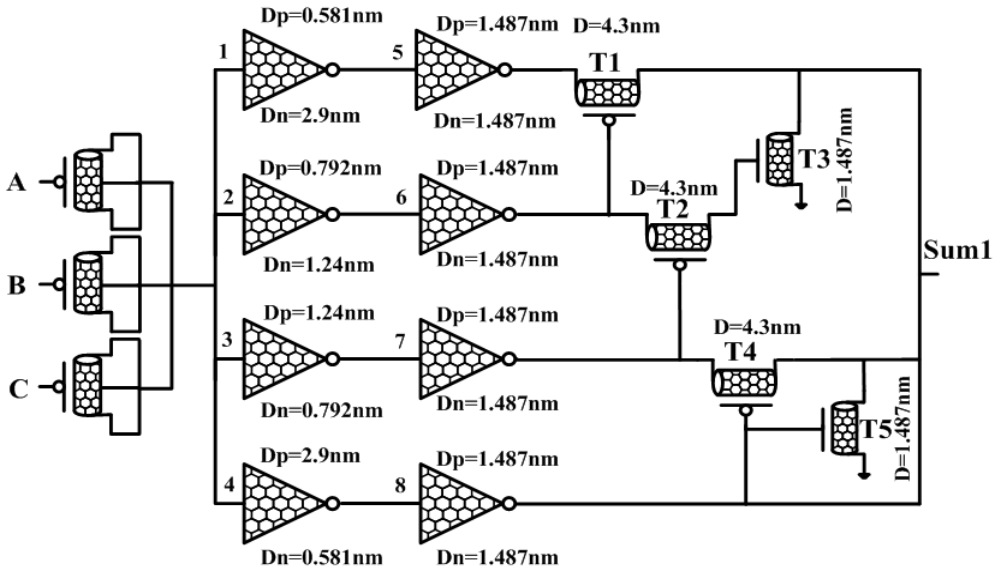

Fig 6. The Sum1 generator circuit

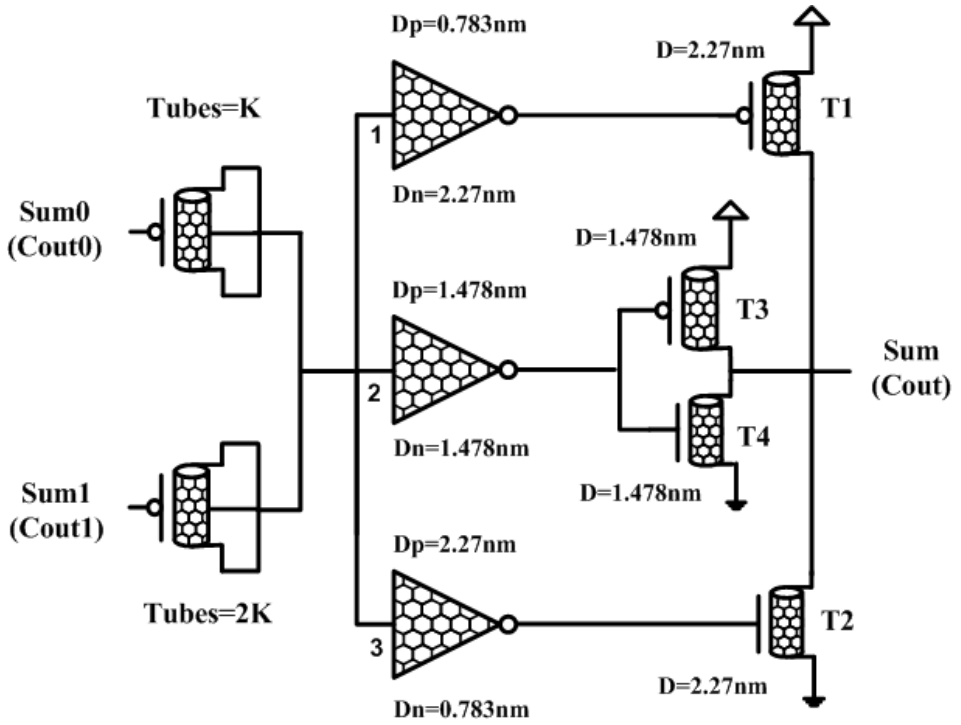

Fig 7. The Binary to Quaternary converter design

When the sum of the inputs is 4 or 5, the output of the first two inverters is 0 and for the other two input inverters is V_{DD}. Therefore, the voltage level at the output of 5 and 6 is V_{DD} and at the output of 7 and 8 is 0. As a result, T1 is OFF, T2 and T3 are ON and consequently Sum1 would be 0. Moreover, if the sum of the input values is 6 or 7, the output of first three inverters is 0 and the output of the fourth one is V_{DD}. Accordingly, T1, T2 and T3 are OFF and T4 is ON and consequently Sum1 is V_{DD}. Finally if the summation of the inputs is above 7, the outputs of all the inverters would be 0 and T5 is ON and accordingly Sum1 would be 0.

C. Binary to Quaternary converter

In the last step of the proposed quaternary full adder cell a binary to quaternary converter, shown in Fig 7, is designed in order to generate quaternary outputs. In this circuit two capacitors with different capacitance values are used. The capacitance of the capacitor which is connected to Sum1 or Cout1 is doubled of the capacitor which is connected to Sum0 or Cout0, since the significance of Sum1 and Cout1 digits is twice of the significance of Sum0 and Cout0. Finally, a quaternary buffer is used in order to boost the driving capability and restore the output voltage level [13].

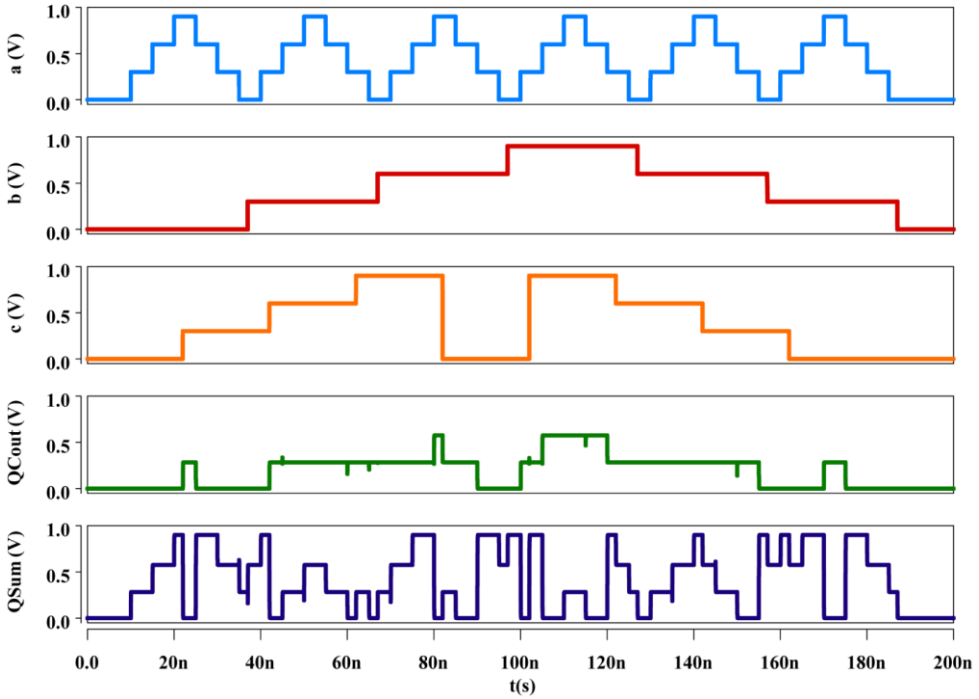

Fig 8. Input and output transient patterns

IV. Simulation Results

In this section simulation results of the proposed quaternary full adder are presented. The Synopsys HSPICE simulator with the compact SPICE model for CNTFETs is used for the simulations at 32nm technology node [14]-[16]. This model is designed for unipolar MOSFET-like CNTFET devices and each transistor can have one or more CNTs under its gate.

Simulations are conducted at 0.9V and 1V power supplies, at different temperatures and with different load capacitors. The delay of each circuit is calculated from the time that the input signal reaches the half of its voltage level to the time that the output signal reaches the half of its voltage level. The average power consumption is also considered as the power consumption parameter.

The transient response of the proposed design is demonstrated in Fig 8. It shows the correct operation of the proposed quaternary full adder. Figures 9, 10 and 11 show the delay, power consumption and PDP of the proposed quaternary full adder with different load capacitors. Also fig 12 shows the PDP variations of the proposed quaternary adder against temperature variations.

Table 2. Simulation results of the proposed circuit

Supply voltage (V_{DD})	Delay (x 10^{-12} s)	Power (x 10^{-5} W)	Power Delay Product (PDP) (x 10^{-15} J)
0.9	*112.76*	*7.5347*	*8.4959*
1	*90.256*	*9.9963*	*9.0223*

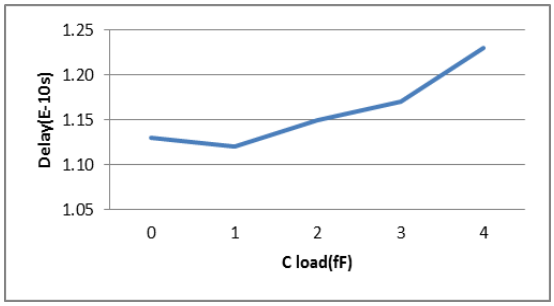

Fig 9. Delay of the proposed circuit versus load capacitance variation

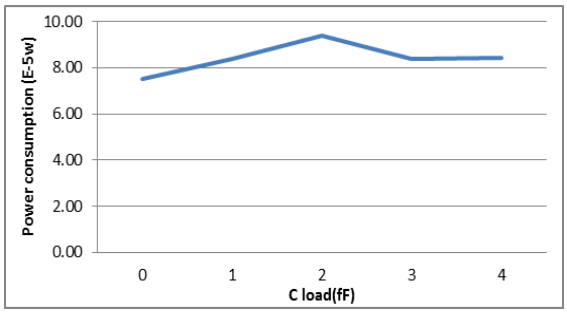

Fig 10. Power of the proposed circuit versus load capacitance variation

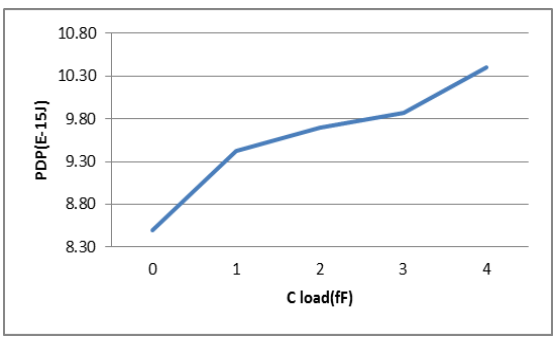

Fig 11. PDP of the proposed circuit versus load capacitance variation

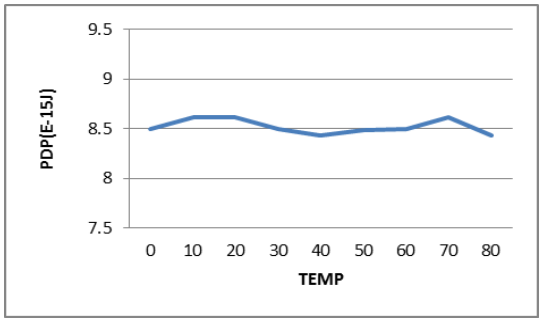

Fig 12. PDP of the proposed circuit versus temperature variation

V. Conclusion

In this article, a high performance CNTFET based quaternary full adder cell has been proposed. As the threshold voltage of the CNTFET is related to the geometry of the CNTFET (DCNT), a new multi-diameter and consequently multi-threshold voltage CNTFET based quaternary full adder design has been introduced in this paper. Proposed quaternary full adder is designed with quaternary to binary converter, sum and carry generator and binary to quaternary converter. All simulations have been performed in HSPICE using the CNTFET model at 32nm technology node.

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