

# Study of Recent Charge Pump Circuits in Phase Locked Loop

**Umakanta Nanda, Jyotirmayee Sarangi, Prakash Kumar Rout**

Department of Electronics and Communication Engineering, Silicon Institute of Technology, Bhubaneswar, India  
Email: uk\_nanda@yahoo.co.in, sarangijyotirmayee604@gmail.com, prakash@silicon.ac.in,

**Abstract**—This paper reviews the design of phase locked loop (PLL) using recently reported charge pump circuits. Lock time, phase noise, lock range and reference spur of each charge pump circuit are investigated. Though improved charge pump circuits are designed recently, their performance is not as effective as the basic charge pump PLL (CP-PLL). Initially the design of PLL using the basic charge pump is completed in this paper and then the PLL using improved charge pumps are redesigned in CMOS 180 nm technology and simulated using Cadence Virtuoso Analog Design Environment. Finally all the charge pumps are compared with respect to the PLL performances. The current starved voltage controlled oscillator (VCO) used for the design of PLL brings about a tuning range of 119.5 MHz to 2.3 GHz. The PLL using different charge pumps produces a lock time which varies from 204 ns to 329 ns. The other parameters like lock range, phase noise and reference spur are also examined.

**Index Terms**—Lock in time, lock range, phase noise, Phase locked loop (PLL), reference spur, Voltage controlled oscillator (VCO).

## I. INTRODUCTION

The heart of almost all modern communication systems is phase locked loop (PLL). A PLL [1] is a type of closed loop system that aids in synchronization of the phase of feedback signal to the reference signal. This synchronizing state is referred to be the lock state of PLL. Locking means a zero phase difference between two signals but if it is considered practically, a small error or offset in phase of the output signals always exists. The PLL block diagram is shown in Fig.1.

The block diagram of PLL is comprised of five components which are phase frequency detector (PFD), charge pump, loop filter, voltage controlled oscillator (VCO) and frequency divider.

In this paper various designs of improved charge pump circuits leading to better performance by the overall PLL is studied.

The charge pump [2] with the help of leakage current, delay offset and the mismatch in the PFD are analyzed in a quantitative manner. In order to choose an appropriate charge pump in different PLL applications, multiple architectures are inspected and their performance parameters are examined.

Reference spur is one of the major problem in PLL. In order to suppress the magnitude of reference spur in the output of PLL, a ratioed current charge pump [3] has been introduced. It is implemented by resizing the source and drain network of the charge pump. When compared with a conventional charge pump, it results in a phase noise improvement of 4dBc/Hz. It helps in improving the magnitude of the reference spur also.

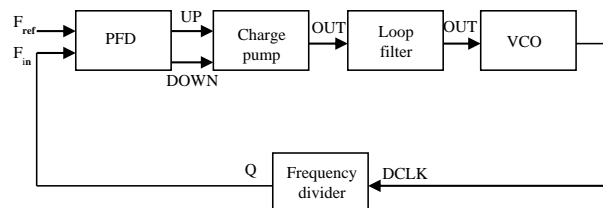


Fig.1. Block Diagram of PLL [1]

The charge pump designed by Hwang et al. [4] helps in minimizing the mismatch enclosed by the charging and discharging currents. Across a wide range of output voltage, the current always remains constant. The matching of the current helps in reducing the static phase offset. The constant current also helps in controlling the dynamics of PLL accurately.

Another charge pump [5] has been introduced for reduction of mismatches between up and down currents. It uses a single two stage amplifier. The amplifier not only helps in reducing the mismatches but also it helps in steering of current.

In order to minimize the variation of the current over a wide range of output voltage a charge pump designed by Liu et al. [6] has been implemented. Here the charge pump loop bandwidth remains constant. It also helps in maximizing the dynamic range.

The basic charge pumps usually have UP and DOWN switches. These switches are made up of PMOS and NMOS. When charge is dumped into the loop filter, the gain boosting charge pump [7] helps in mismatching of the current which generally occurs due to the difference between source and drain voltages of the PMOS and NMOS. However it requires more transistors as compared with the conventional charge pump.

Due to the current mismatch which is one of the common problems in conventional charge pump, the phase noise of overall PLL is dominated. A high performance charge pump circuit [8] is used for

eliminating the this problem of current mismatch. In this design, a rail to rail operational amplifier is introduced. The reference circuit and self biasing cascode current mirror switch on the current of the charge pump, so that it can be matched in a wide range of output voltage.

To reduce current mismatch, a typical type of transmission gate cascode current mirror(TGCCM) charge pump [9] is designed. It consists of one supply reference current source which is independent. In order to reduce switching errors, a switching technique is used named as transmission gate switching. The control voltage which is obtained when the PLL locks is free from ripples. It also helps in reducing the reference spur.

The charge pump designed by Yuan et al. [10] solves the problem of current mismatching by introducing a replica biasing technique. This structure produces a constant current stable operation. It consists of charge pump core circuit and a feedback network. The inverting input terminal of the feedback network is merged with the output of the core charge pump. Similarly the non-inverting input terminal of the feedback network is connected to the output of replica bias circuit. The output of the operational amplifier is used for biasing the charge pump discharging current.

The general charge pump circuits have some small amount of current mismatching characteristics. This current mismatch produces a phase offset which results in increasing reference spur in the PLL output signal. In general, it also reduces the locking range of PLL. With an account of introducing error amplifier and reference current sources, the charge pump designed by Lee et al. [11] helps in reducing the mismatch problems. It also helps in achieving a charge pump with best current matching characteristics.

In the charge pumps discussed earlier, the reference current depends upon the supply voltage. Therefore, it can be sensible for the power supply noise. The charging and discharging currents of the charge pump is influenced by the power supply noise. The charge pump [12] with a beta-multiplier circuit uses a differential amplifier. In this case the reference current is nearly independent of supply voltage. Using a bias circuit it produces bias voltages for the folded cascade circuit.

A typical structure of charge pump circuit [13] is introduced, where the current flow technology is used. The technology is used for making the perfect current matching characteristics. In this design two differential inverters are built-in for increasing the speed of the charge pump.

A charge pump [14] calibration technique designed by Chiu et al. is used for a delta-sigma fractional-N phase locked loop. An auxiliary path is introduced to this circuit. By utilizing some amount of interval in a period of reference cycle, the mismatch is detected. As a result, the difference in current of UP/DOWN is corrected.

The charge pump circuit designed by Umezawa et al. [15] has a concept which is similar to the Dickson charge pump circuit. The Dickson charge pump circuit states that, in order to eliminate the threshold drop problem, four

phase clocks are utilized. It controls the gate voltage of the charge pump which is transferred to the devices.

A bootstrapped circuit [16] and an auxiliary circuit [17, 18] were used in a charge pump, so that they could elevate the voltage of Dickson voltage multiplier which is pumped. These circuits are dwelled with more silicon area in such a way that, extra power is wasted in the system.

In order to design a low voltage differential signalling (LVDS) serializer/deserializer (SerDes), a charge pump designed by Pan et al. [19] has been introduced. In a traditional charge pump, non ideal effects like clock feed-through, charge sharing and current mismatch are common. This design can reduce such type of effects using wide swing cascode current mirrors.

Section II discusses the components of PLL. Since the invention, it has become a challenging work for the designers to build a fast, low noise, and wide range PLL. Clock generation [20] and clock recovery in microprocessors are the most important applications of PLL. Phase locked loop are mainly used for synchronization and frequency synthesis. Recent market demand for communication systems which use frequency in the range of GHz and hence PLL work for same frequency range with less lock time and low noise. There are lots of challenges in the design of PLL but one of them is to produce low phase noise oscillator by using CMOS technology. Power consumption [21] of any analog and mixed signal circuits cannot be neglected. The aspect of PLL is encapsulated in this paper by using CMOS technology in cadence design environment. Section III involves in results of basic charge pump PLL (CP- PLL). Section IV presents the recent charge pumps and their performance comparison. Section V finally presents the concluding remarks.

## II. PLL COMPONENTS

Basically various types of PLL are available serving different applications. Some of the considerable PLL are linear PLL, digital PLL and analog PLL. The linear operations of the PLL includes linear baseband model, transfer functions, PLL with active loop filter, stability considerations etc. The analog PLL are used in a wide range of application, but the digital PLL are more attractive and giving more attention for the betterment of digital systems. The advantage in using digital PLL is that it produces a good speed, reliability and low cost. If we consider, a comparison which occurs between analog signal and digital signal, digital PLL are very good in operating at low frequencies but analog PLL has a big problem in operating at low frequencies. A very well known error detectors are used in analog PLL, which in result are very sensible to D.C. drifts. Such type of difficulty does not arise in digital PLL. The PLL which is used in this paper is a mixed signal type of PLL (Fig.1). The basic components of this PLL are discussed below.

### A. Phase frequency detector

The block diagram of PFD is shown in Fig.2. The phase frequency detector [22] shown in Fig.2 is a conspicuous component of PLL. This PFD is having two inputs  $F_{ref}$  and  $F_{in}$ . Depending upon the deviation of the phase of these two signals, UP and DOWN signals are generated. The PFD block diagram consists of one AND gate and two edge triggered D flip flops. The D input is coupled to logic 1. The reference input  $F_{ref}$  and feedback input  $F_{in}$  represents the two inputs of the flip flops. The AND gate is connected to the reset of each of the flip flop. If the reference input rising edge leads the feedback input, UP signal goes high and DOWN signal goes low. If the feedback input goes high UP signal goes low and DOWN signal goes high.

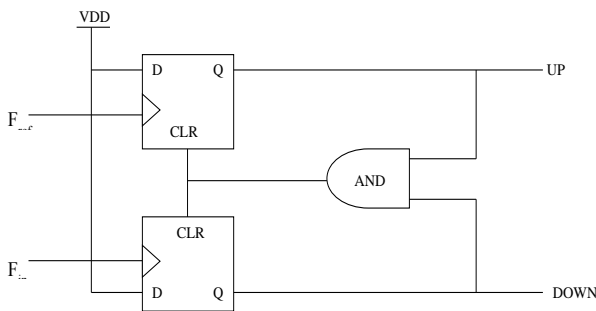


Fig.2. PFD block diagram [22]

**B. Charge pump**

The phase frequency detector output UP and DOWN are required to be combined into single input for driving the VCO. This process can be fulfilled by a circuit known as charge pump. The charge pump [23] is a sensible component of PLL. It compares the phase difference between  $F_{ref}$  and  $F_{in}$  and produces an equivalent voltage for tuning the VCO. The charge pump of PLL is considered to be ideal when it produces equal output current from both the UP and DOWN network. Eventually single output current is pumped out from this circuit by taking two input voltages UP and DOWN. The schematic of a basic charge pump [24] circuit is shown below in Fig.3.

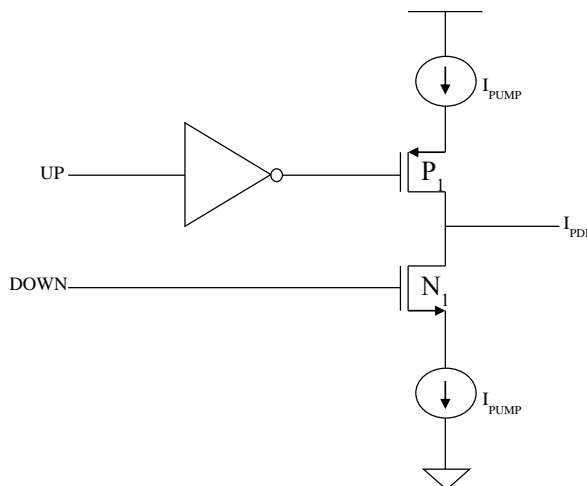


Fig.3. Charge pump circuit [24]

In the above figure the both current sources  $I_{pump}$  is placed in series with the transistors. When input signal UP is high the  $P_1$  transistor goes ON. The resultant current  $I_{PDI}$  results in positive polarity. When DOWN is high making  $N_1$  transistor active, The resultant current  $I_{PDI}$  results in negative polarity. The output current  $I_{PDI}$  can be written as,

$$I_{PDI} = \frac{I_{pump} - (-I_{pump})}{4\pi} \cdot \Delta\phi = K_{PDI} \cdot \Delta\phi \quad (1)$$

where  $\Delta\phi$  is the phase difference, and

$$K_{PDI} = \frac{I_{pump}}{2\pi} \text{ (amps/radians)} \quad (2)$$

**C. Loop filter**

It is important to symbolize that the output converted from phase frequency detector and charge pump is comprised of high dc frequency components with a considerable amount of ac components. Hence loop filter has been introduced for filtering those ac components. The loop filter [25] is a passive type low pass filter. For maintaining the stability loop filter is used as a vital component. Ideally the low pass filter helps in maintaining a constant voltage which is provided to the input of VCO. The loop filter schematic is shown below in Fig.4.

For adjustment of the VCO frequency, the loop filter provides the required control voltage. When the charge pump starts driving the R and  $C_1$ , a current enters into the filter and the control voltage start experiencing the jump, hence a jump in output frequency of VCO. So to reduce this effect a second capacitor  $C_2$  is made in parallel to the resistor. Ideally  $C_2$  is made  $1/10^{th}$  of  $C_1$ .

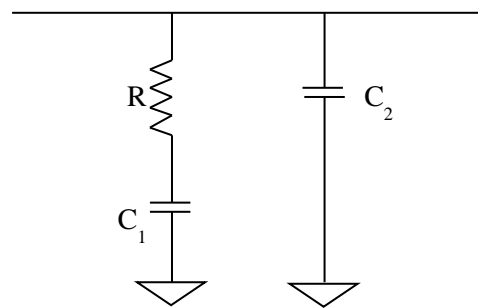


Fig.4. Loop filter [25]

**D. Voltage controlled oscillator**

The VCO [26] is also a crucial component of PLL. Especially where the control voltage of charge pump drives the VCO output frequency for synchronization with the reference signal frequency. The principle of oscillator's state that it induces a periodic output which is generally in the form of voltage. The implementation of PLL can be of various types. A current starved VCO of odd number of inverter stages can be used in PLL. The

operating principle of current starved VCO is analogous to ring oscillator. The ring oscillator is adding to be the closed loop cascade connection of inverters. The output node of the last inverter is connected to the input node of the first one. The schematic of VCO is represented below in Fig.5. The transistors  $P_1$  to  $P_5$  and  $N_1$  to  $N_5$  operate as inverters while transistors  $P_6$  to  $P_{10}$  and  $N_6$  to  $N_{10}$  operate as current sources. The current source act as a cut off point for the availability of the current to the inverter. In other words the inverter stages are starved for current by the current sources. If the time for the charging and discharging of output node is  $\tau$ , then the oscillator frequency is given as,  $f=1/2N\tau$ , where  $N$  represents number of inverters in VCO.

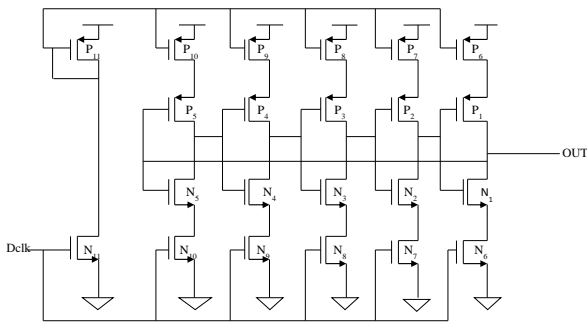


Fig.5. Five stage voltage controlled oscillator [26]

**E. Frequency divider**

The frequency divider [27] is a closed loop circuit which can be implemented by using a D – flip flop. The main goal of frequency divider is that it is used for frequency scaling purpose. The VCO output frequency is divided by the help of a frequency divider so that reference frequency and feedback frequency will be matched. The schematic of frequency divider by 2 circuit is depicted in Fig.6.

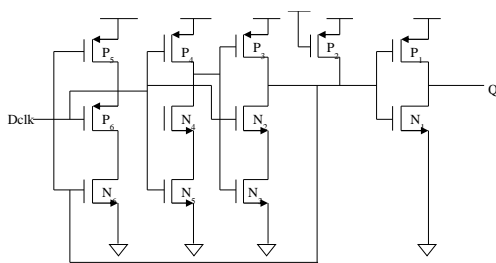


Fig.6. Frequency divider [27]

**III. RESULTS OF BASIC CP-PLL**

The complete PLL is designed using cadence virtuoso tool. The physical layout is depicted in Fig.7. where the area is measured to be  $10.664 \text{ mm}^2$ .

The transient response of basic CP-PLL is demonstrated below in Fig.8. The figure gives a image that feedback input frequency and reference frequency are synchronized.

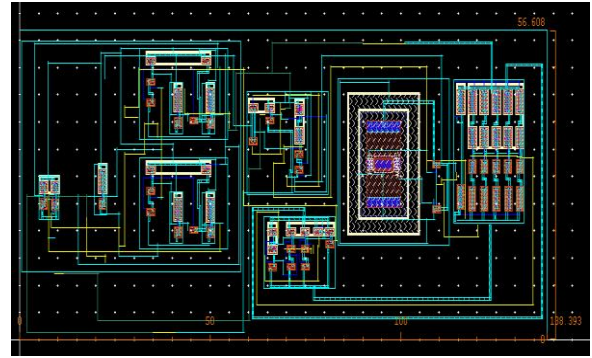


Fig.7. Chip layout of basic CP-PLL

The PLL of 1.8 GHz operating frequency starts to lock at a time of 204 ns which is referred to as lock time. The phase noise variation of this basic PLL is plotted in Fig.9. It is observed that with a rise in operating frequency, the PLL experiences a degraded phase noise. The lock range of this PLL is measured to be 667 MHz to 2 GHz making it suitable for GSM applications.

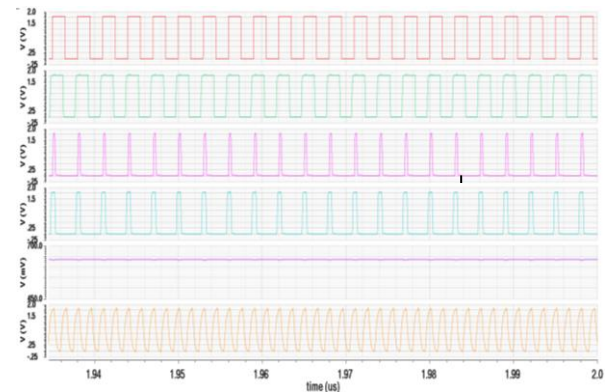


Fig.8. Transient response of PLL in locked state

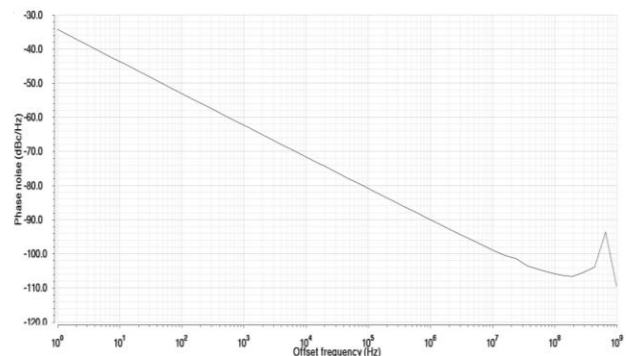


Fig.9. Phase noise variation with offset frequency

**IV. RECENT CHARGE PUMPS AND THEIR COMPARISONS**

This section introduces several recent charge pumps and their comparative analysis carried out for the performances like lock range, lock time, phase noise, reference spur.

A charge pump [28] which is having a very fast output discharging and improved output current matching is

shown below in Fig.10. This is a NMOS – switch high swing cascode type charge pump. At the output stage, the resistance of current mirrors is increased here. The current of the UP network is prepared by the P type transistors  $P_1, P_2, P_5, P_6$  and  $P_7$  and current of the DN network is produced by the N type transistors namely  $N_1, N_2, N_3, N_4$  and  $N_{11}$ . When the output resistance increases the matching of the output current is extremely enhanced. The slow node problem is resolved by a pull up mirror which is introduced in the design of charge pump. For the UP current, the pull up mirror is brought about by the transistors named as  $P_8, P_9$  and  $N_8$ . When UP signal goes low the current present in transistor  $P_5$  falls down to zero. The charge pump current  $I_{cp}$  is mirrored to the transistor  $P_9$  by the transistor  $P_8$  which in turn pulls the transistor  $P_5$  to VDD. Hence  $P_4$  can easily be switched off. The dc current introduced in this work is 80 uA.

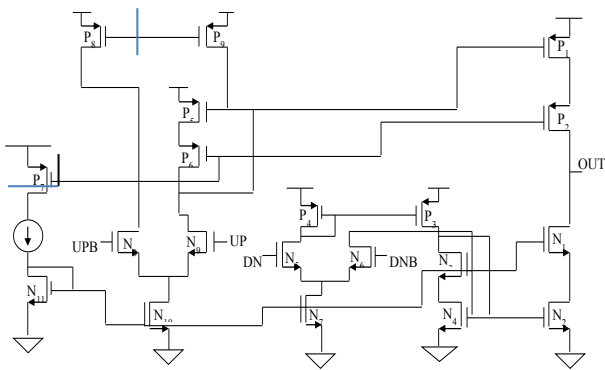


Fig.10. NMOS-switch high swing cascode charge pump [28]

For improvement of the switching speed and minimization of the switching mismatch problem of the charge pumps, the NMOS – switches current steering charge pump has been used. This charge pump [28] is shown below in Fig.11. It comprises of two differential pairs of transistor. These transistors are named as  $MN_4 - MN_5$  and  $MN_6 - MN_7$ . The function of these transistors is that they work as NMOS switches. The operating principle of the circuit in Fig. 11.is as follows. When the signal UP is high, DN signal goes low resulting in, the transistor  $MN_4$  gets ON. It then turns ON the PMOS current mirror transistors,  $MP_1$  and  $MP_2$ . Simultaneously, the transistor  $MN_7$  gets OFF as long as the DN signal is low. The  $MN_3$  current is driven into the  $MN_6$ . In a similar way when the signal UP is low, DN signal goes high.

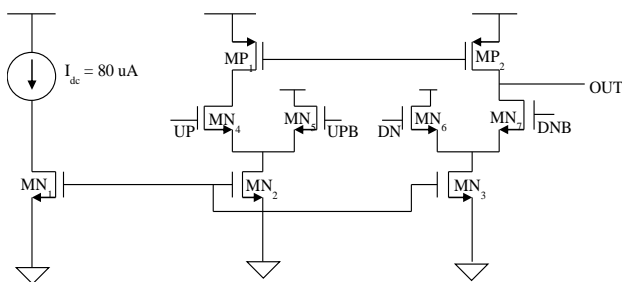


Fig.11. NMOS – switch current steering charge pump[28]

In another work done by Sen et al. [29] charge pump shown in Fig.12. works in the function of converting phase frequency detector signal to the analog signal. The output helps to control the VCO frequency. Fig.12.gives a knowledge that two PMOS and two NMOS are present and connected in series. The  $P_1$  and  $N_2$  are considered to be a current source. The remaining part of the charge pump  $P_2$  and  $N_1$  are biased by UPB and DOWN generated from the PFD output.

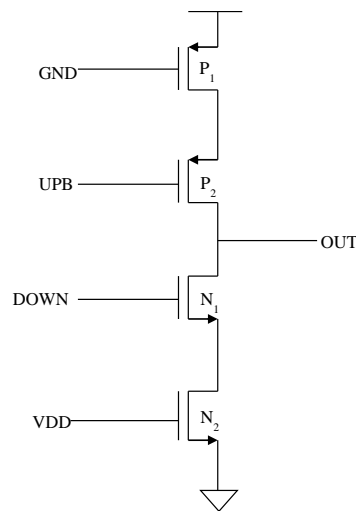


Fig.12. Charge pump circuit [29]

Charge pump primarily transfers both the PFD digital outputs to a single current signal. It helps in maintaining a steady control signal for maintaining the VCO frequency. Charge pump accumulates the charge in the loop filter capacitor. For the reduction of the error signal to a very small value an improved charge pump [30] is used which is shown below in Fig.13. The charge pump is operated by the signals UPB and DN. These signals are generated by the PFD. When  $P_1$  gets ON, UPB goes high. Similarly when  $N_1$  is ON, DN becomes low.

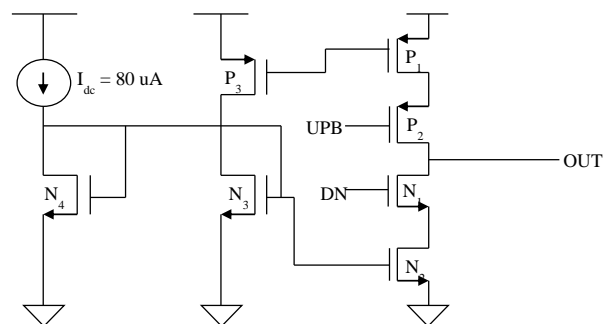


Fig.13. Charge pump circuit [30]

The total time taken by a PLL for capturing a signal is termed as lock time. It is also referred to as acquisition time of PLL. The comparison of the control voltages of the PLL using different charge pumps is shown in Fig.14. The lock time by using the charge pump of section 2, found to be 204 ns which is best among all other charge pumps.

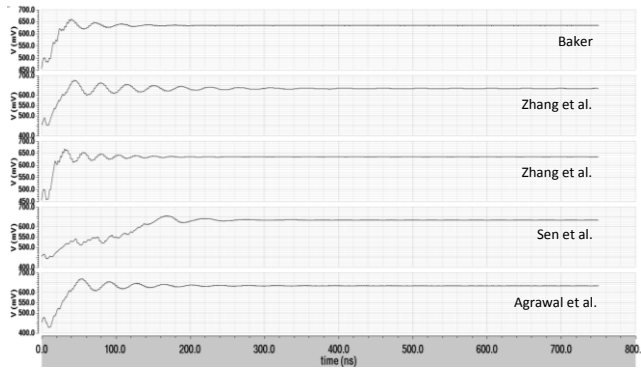


Fig.14. Comparison of control voltage for VCO using different charge pumps

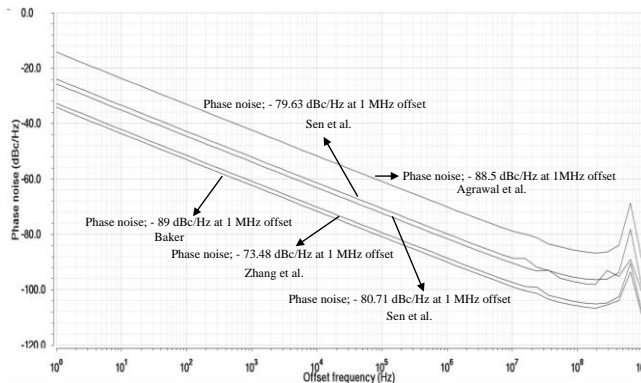


Fig.15. Phase noise variation of PLL using different charge pumps

Table 1. Comparison of PLL performance parameters using different charge pumps

Parameters	Basic CP-PLL	[28]	[28]	[29]	[30]
Lock time (ns)	204	706	269	259	329
Lock range (GHz)	0.667- 2	0.661- 1.9	0.665- 1.97	0.649- 1.2	0.662- 1.95
Phase noise (dBc/Hz) at 1 MHz offset	-89	-73.48	-80.71	-79.63	-88.5
Reference spur(dBc/Hz) at 1 MHz offset	-101	-83	-92	-89	-99.12

V. CONCLUSION

Lock time, lock range, phase noise and reference spur of PLL using different charge pumps are analyzed and demonstrated in this paper. Further the comparison among these performances of different charge pumps is demonstrated. For maintaining the stability of lock time of the loop filter, PFD architecture can be an important factor. The current of the charge pump should be properly adjustable. The center frequency of VCO can vary and depending upon the loop filter components. Some improved PLLs are also simulated using Cadence Virtuoso 180 nm CMOS technology. The lock range

generated by the basic CP-PLL is 661 MHz – 2 GHz which is proved to be better as compared to the improved charge pumps. The basic CP-PLL generates a large tuning range of 119.5 MHz – 2.3 GHz. and produces a fast locking time of 204 ns where the phase noise is -89dBc/Hz at 1 MHz offset frequency and reference spur is -101dBc/Hz.

The phase frequency detector output UP and DOWN is required to be combined into single input for driving the loop filter. This process can be fulfilled by a circuit known as charge pump. The charge pump [1] is a sensible component of PLL. It compares the phase difference between  $F_{ref}$  and  $F_{in}$  equivalent

REFERENCES

- [1] Chen, Yuanfeng, Pui-In Mak, and Yangzhong Zhou. "Self-tracking charge pump for fast-locking PLL." *Electronics letters* 46.11 (2010): 755-757, 27th May 2010, Vol. 46 No. 11.
- [2] Rhee, Woogeun. "Design of high-performance CMOS charge pumps in phase-locked loops." *Circuits and Systems, 1999. ISCAS'99. Proceedings of the 1999 IEEE International Symposium on*. Vol. 2. IEEE, 1999.
- [3] N. Kamal, S. F. Al-Sarawi and D. Abbott, "Reference spur suppression technique using ratioed current charge pump," in *Electronics Letters*, vol. 49, no. 12, pp. 746-747, June 6 2013. doi: 10.1049/el.2013.1010
- [4] Hwang, M-S., Jaeha Kim, and D-K. Jeong. "Reduction of pump current mismatch in charge-pump PLL." *Electronics Letters* 45.3 (2009): 135-136.
- [5] Fazeel, H. Md Shuaeb, et al. "Reduction of current on VLSI mismatch in PLL charge pump." *2009 IEEE Computer Society Annual Symposium*. IEEE, 2009.
- [6] Liu, P., et al. "PLL charge pump with adaptive body-bias compensation for minimum current variation." *Electronics letters* 48.1 (2012): 16-18.
- [7] Choi, Y-S., and D-H. Han. "Gain-boosting charge pump for current matching in phase-locked loop." *IEEE Transactions on Circuits and Systems II: Express Briefs* 53.10 (2006): 1022-1025.
- [8] Zhiquan, Li, Zheng Shuangshuang, and Hou Ningbing. "Design of a high performance CMOS charge pump for phase-locked loop synthesizers." *Journal of Semiconductors* 32.7 (2011): 075007.
- [9] Umakanta Nanda, Debiprasad Priyabrata Acharya, and Sarat Kumar Patra. "A new transmission gate cascode current mirror charge pump for fast locking low noise PLL." *Circuits, Systems, and Signal Processing*, 33.9 (2014): 2709-2718.
- [10] Sun, Yuan, Liter Siek, and Pengyu Song. "Design of a high performance charge pump circuit for low voltage phase-locked loops." *2007 International Symposium on Integrated Circuits*. IEEE, 2007.
- [11] Lee, Jae-Shin, et al. "Charge pump with perfect current matching characteristics in phase-locked loops." *Electronics Letters* 36.23 (2000): 1907-1908.
- [12] Hieu, Ngo Trong, Tae-Woo Lee, and Hyo-Hoon Park. "A perfectly current matched charge pump of CP-PLL for chip-to-chip optical link." *Conference on Lasers and Electro-Optics/Pacific Rim*. Optical Society of America, 2007.
- [13] Juarez-Hernandez, Esdras, and Alejandro Diaz- Sanchez. "A novel CMOS charge-pump circuit with positive feedback for PLL applications." *The 8th IEEE International Conference on Electronics, Circuits and*

- Systems, ICECS*. Vol. 1. 2001.
- [14] Chiu, Wei-Hao, Tai-Shun Chang, and Tsung-Hsien Lin. "A charge pump current mismatch calibration technique for  $\Delta\Sigma$  fractional-N PLLs in 0.18- $\mu\text{m}$  CMOS." *Solid-State Circuits Conference, 2009. A-SSCC 2009. IEEE Asian. IEEE*, 2009.
- [15] Umezawa, Akira, et al. "A 5-V-only operation 0.6- $\mu\text{m}$  flash EEPROM with row decoder scheme in triple-well structure." *IEEE Journal of Solid-State Circuits* 27.11 (1992): 1540-1546.
- [16] Sawada, Kikuzo, Yoshikazu Sugawara, and Shoichi Masui. "An on-chip high-voltage generator circuit for EEPROMs with a power supply voltage below 2 V." *VLSI Circuits, 1995. Digest of Technical Papers., 1995 Symposium on. IEEE*, 1995.
- [17] Lin, Hongchin, Kai-Hsun Chang, and Shyh-Chyi Wong. "Novel high positive and negative pumping circuits for low supply voltage." *Circuits and Systems, 1999. ISCAS'99. Proceedings of the 1999 IEEE International Symposium on*. Vol. 1. IEEE, 1999.
- [18] Lai, Sheng-Yeh, and Jinn-Shyan Wang. "A high-efficiency CMOS charge pump circuit." *Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on*. Vol. 4. IEEE, 2001.
- [19] Pan, Jianbin, and Yuanfu Zhao. "Design of a Charge-Pump PLL for LVDS SerDes." *International multi conference of Engineers and Computers Scientists*. Vol. 2. 2010.
- [20] Mohanty, Sudatta, Madhusmita Panda, and Ashis kumar Mal. "Design and Performance Analysis of a Phase Locked Loop using Differential Voltage Controlled Oscillator." *International Journal of Scientific & Engineering Research*, Volume 5, Issue 5, May-2014 45 ISSN 2229-5518.
- [21] Bilal A. Shehada, Ahmed M. Serdah, and Aiman Abu Samra. "Enhancing Leakage Power in CPU Cache Using Inverted Architecture." *International Journal of Modern Education and Computer Science* 5.2 (2013): 12.
- [22] Kasht, Swati, et al. "Designing of Charge Pump for Fast-Locking and Low-Power PLL.", *International Journal of Computer Technology and Electronics Engineering (IJCTEE)*, Volume 2, Issue 6, 2012.
- [23] Talwekar, R. H., and S. S. Limaye. "Design of high gain, high bandwidth Op-Amp for reduction of mismatch currents in charge pump PLL in 180 nm CMOS technology", *World Acad. Sci. Eng. Technol*, pp. 590-593, 2010.
- [24] Terlemez, Bortecene, and John P. Uyemura. "The design of a differential CMOS charge pump for high performance phase-locked loops", *Proceedings of the 2004 International Symposium on Circuits and Systems*, Vol. 4, 2004.
- [25] Baker, R. Jacob, *CMOS: circuit design, layout, and simulation*. Vol. 1. John Wiley & Sons, 2008.
- [26] Goyal, Bhavana, ShrutiSuman, and P. K. Ghosh. "Design of Charge Pump PLL using Improved Performance Ring VCO", *International Conference on Electrical, Electronics, and Optimization Techniques (ICEEOT) – 2016*.
- [27] U. Nanda, D. P. Acharya and S. K. Patra, "Design of a low noise PLL for GSM application," *International conference on Circuits, Controls and Communications (CCUBE), 2013, Bengaluru, 2013, pp. 1-4*.
- [28] Cheng Zhang, Thomas Au, Marek Syrzycki. "A high performance NMOS-switch high swing cascode charge pump for phase-locked loops", *55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2012.
- [29] Sen, Yashpal, and Nitin Jain. "Design and Implementation of Phase Locked Loop Using Current Starved Voltage Controlled Oscillator." *Advance in Electronic and Electric Engineering*. ISSN: 2231-1297.
- [30] Agrawal, Anshul, and Rajesh Khatri. "Design of Low Power, High Gain PLL using CS-VCO on 180nm Technology." *International Journal of Computer Applications* 122.18 (2015).

### Authors' Profiles



**Umakanta Nanda** received MTech degree in Electronics and Communication engineering from National Institute of Technology, Rourkela, India, and is currently perusing PhD in the area of Analog and mixed signal VLSI designs at National Institute of Technology, Rourkela, India. His research interests is analog and mixed signal integrated circuits and application specific processor design, and embedded systems design.



**Jyotirmayee sarangi** was born in the year 1992, Oct 16. She has completed her 10<sup>th</sup> from Nirmala Convent School, Keonjhar. Her 12<sup>th</sup> was from DD autonomous college, Keonjhar. She has got her BTech degree from Purushottam Institute of Engineering and Technology, Rourkela in the department of Electronics and Telecommunication Engineering. Presently she is continuing her MTech in electronics and communication in silicon institute of technology.



**Prakash Kumar Rout** received M.Tech degree in communication system engineering from Kalinga Institute of Industrial Technology, Bhubaneswar, India, in 2008 and Ph.D. degree in the department of Electronics and Communication Engineering, National Institute of Technology, Rourkela, India. His research interests include analog and mixed signal integrated circuits and computational intelligence.