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Optimized Low Power Dual Edge Triggered Flip-flop with Speed Enhancement

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Abstract: This paper gives a novel low-power approach with pulse generating circuits using dual edge triggered flip-flops. By doing so, flip-flop might operate at 1.2Volts, with the novel quick latch and conditional precharging.

This paper aims at a new proposed low power dual edge triggered flip-flop with speed enhancement to achieve low power consumption with a shorter delay in power usage, hence, it is well suited for low-power digital system applications. The new proposed low power dual edge triggered flip-flop also aims at comparison with the three DETFF, Static Output Controlled Discharge Flip-Flop (SCDFF), Dual Edge Triggered Static Pulsed Flip-flop (DETSPFF), and Pervious work on Dual Edge Triggered flip-flop, proves to achieves with reduction in numbers of transistors in the stack and increases the number of charge-paths results in a faster operational speed. According to simulation on Spectre simulator, it has been observed that total power consumption of proposed flip flop at 0.67 switching activity is 30.16 % and 27.36 % less than that of previous arts DSPFF and SCDFF respectively. Clock-gated sense-amplifier is incorporated to reduce power consumption at low switching activity. The simulation is done using Cadence tool with 45nm standard CMOS technology.

Index Terms: Dual Edge Triggered (DET), DETFFs (double-edge-triggered flip-flops), Dual Edge Triggered Static Pulsed flip-flop (DETSPFF), Static output Controlled Discharge Flip-flop (SCDFF), FF (Flip-Flop), Single Edge Triggered (SET), Sense Amplifier (SA), VLSI (Very large scale integration).

1. Introduction

The clock matrix constitutes clock distribution networks and FF are the most potent hungry components for numerous VLSI digital systems.

It consumes thirty percent to sixty percent of total system power with the FF's & the final divisions of the clock distribution network driving flip-flops using 90 percent of that. The system power division of clocking can be supplementary evident as a result of the new generation frequency scaling and extensive pipelining. Because today's portable digital circuits have a restricted power budget, it's critical to reduce the power dissipation in clock network and flip-flops.

There are several ways to reduce clock power. The most influential way is V_{dd} scaling, which has quadratic impact on PcIk' However, V_{dd} has already been reduced along with downscaling of process. The capacitance is unlikely to decrease as long as the number of transistors in a circuit becomes larger and functionality is more complex. One effective way to reduce f_{Clk} without performance degradation is to use dual edge-triggered flip-flops (DETFFs). The cross DETFF requires only half of f_{clk} to maintain the same throughput as single edge-triggered flip-flop (SETFF). Two main categories of DETFFs are master slave and pulse triggered. They put positive and negative flip-flops in parallel to perform dual edge triggering. These structures are straightforward. However, the internal are charging and discharging at every clock cycle regardless of the input even when they are sampled at the same value. This wastes a lot of power. Pulse triggered flip-flop is used for low power consumption.

The paper discussion organizes in following manner. The previous work on dual edge triggered flip-flops (DETFF) is reviewed, the structure and operating principal of proposed design, simulation results are presented and in last, we draw conclusion in the final section.

Furthermore, flip-flops delays compelled to reduce because to the restricted timing budget during high frequency operation. As a result, with current VLSI technology, the potential to establish a trade-offs between low-power dissipation and low-latency is critical.

Dual-edge triggering is a significant approach for lowering the clock distribution network's power usage. Because the flip-flop uses dual-edge triggering, it may sample info on falling and rising edges as regards the clock, using just half of the clock frequency to provide the identical data output as SETFF.

2. Related Work

"A dual edge triggered flip-flop by using clock branch sharing scheme."

In this flip-flop design, two latching stages share the clock allocation network to capture and deliver the input data. Clock branch-sharing scheme decreases the number of clocked transistors in the model. The projected design also employs conditional discharge and split path techniques which further help to reduce the short-circuit currents during the switching activity.

"Dual edge triggered D flip flop by introducing efficient explicit clock pulse generator."

The dual edge clocking is achieved by explicit clock pulse generation network. This design avoids the stacking of MOS transistors, reduces internal node switching activity. This flip flop uses minimum number of clocked transistors and overcomes the drawbacks of dynamic logic family with improved delay and power delay product parameters.

"New static based logic flip-flop"

In order to reduce power consumption and glitch reduction to dynamic circuits of dual edge-triggered flip-flop that consists of no pre-charging and conditional discharging when the fan-in is small, this makes the static logic more superior than the conventional method. In this work the flip-flop consumes the least power in spite of the input data activity which in turn reduces the power dissipation of the circuit.

The previous article [1], two DETFF designs for low PDP were presented. To transfer data, proposed1 DETFF utilises a pass transistor, wherein proposed2 DETFF flop uses a transmission gate. To transmit data across the transmission gate, one more inverter was required in proposed2 DETFF, which increased the layout space as well as the power consumption.

This article [2] describes a low power novel-(DETFF) architecture using the 180nm CMOS technology. When compared to SETFF, DETFF can achieve the similar-data throughput with half the clock frequency (SETFF). The traditional and suggested DETFFs are given and compared in this study under the identical simulated settings. When compared to SCDFF, DEPFF, and SEDNIFF, average power dissipation improves by 48.17 percent, 41.29 percent, and 36.84 percent, respectively, while PDP improves by 42.44 percent, 33.88 percent, and 24.69 percent. As a result, the DETFF design described here is well suited to low power and small area applications.

The study [3] highlights the need for a better memory unit that can maintain the state of operation for transiently powered. Systems while also reducing latency and increasing energy economy. The designs are tested for applicability for energy harvesting applications by using clock and power gate.

The proposed [4-5] CBS IP sample the clock transitions using a clock branch sharing in which efficiently lowers the amount of clocked transistors and resulting in reduced-power while retaining the competitive speed. To decrease redundant switching activity and short circuit current, it utilises the conditional discharge approach and the split-path-technique. The CBS IP FF contains the fewest clocked transistors and consumes the least amount of power, making it ideal for usage in both high-performance and low power applications. They work in conjunction with. DETFF, which responds to both positive edges and negative edges, to FF further enhance operating speed while lowering power consumption.

In terms of power consumption and PDP, this architecture improves by up to 20% and 12.4 percent, respectively fewest clocked transistors and uses the least amount of power, making it ideal for high-performance and low-power applications works in conjunction with a DETFF, which responds to both positive and negative edges, to enhance operating speed while lowering power dissipation. In terms of power dissipation, this architecture improves by up to 20% and 12.4 percent, respectively [6].

The design [7-9] of a novel Explicit pulse DET data FF was given in this work. This FF uses less electricity since it has less redundant switching and short current. The FF also contains the fewest number clocked transistors and consumes the least amount of power, making it ideal for usage in both high-performance and low power applications. Furthermore, it is capable of embedding logic functions and more effectively conducts charge sharing free operations [10-15].

3. Static Output-Controlled Discharge FF(SCDFF)

Fig. 1 shows the Pulse Generator for SCDFF. Short pulses are generated at positive edges and negative edges of the input clock CLK.

Fig. 2 represents static latch operates with the pulses generated at every edge of clock in pulse generator circuit. This circuit is design targeting a 45nm technology library.

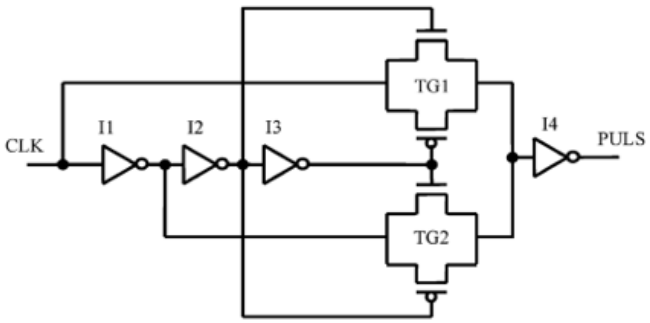

Fig.1. A Pulse Generator

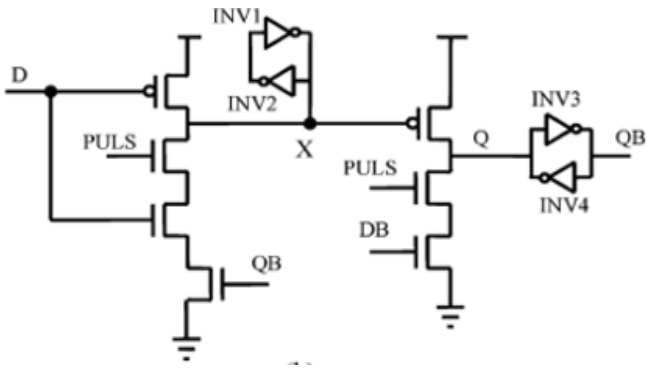

Fig.2. Static Latch

SCDFF comprises of pulse generator along with the static latch that functions in sync with the pulse input signal. The pulse generator initiates pulses at the clock's positive edges and negative edges. There are two static stages in Latch. With a D controlled transistor, one stage goes with pre-charges the node X. In the discharge going path of node X, a QB controlled transistor is employed to implement the conditional discharge technique. It prevents node X from being discharged when the input is high. Node X discharges when the pulse arrives during charging of Q. A pulse-controlled transistor offers a discharge channel for node X during discharging. SCDFF has a number of advantages, including low power dissipation and a soft edge feature. Owing to latch of the single-ended, delay always exists between Q and QB. When the input is low, the static power dissipation in one stage of the latch is higher.

The whole design of Static Output Controlled Discharge Flip-flop is operated at 1 volt. Clock generator is also operating at 1 volt. The rise time t_r is 100 picosec the remaining part is the flip-flop. The pulse from the Pulse Generator is going to trigger the flip-flop at both positive as well as negative edges

3.1. Implementation of Static Output-controlled Discharge FF

A test bench is created to simulate the above design, the test bench carries a clock operates at 50ns and data input D is generated at similar frequency of the clock to eliminate the Setup and Hold time violations of the latch. The transient analysis is carried out with the following parameters.

The Transient Analysis parameters: Stop time: 250ns (D input pattern repeated for two times) V_{bias}: 0.2V.

3.2. Schematic Design of Static Output-controlled Discharge FF

Fig. 3 shows the schematic design of SCDFF which is implemented using above Transient analysis parameters. Fig. 4 shows the Analog simulation implementation of SCDFF using in cadence.

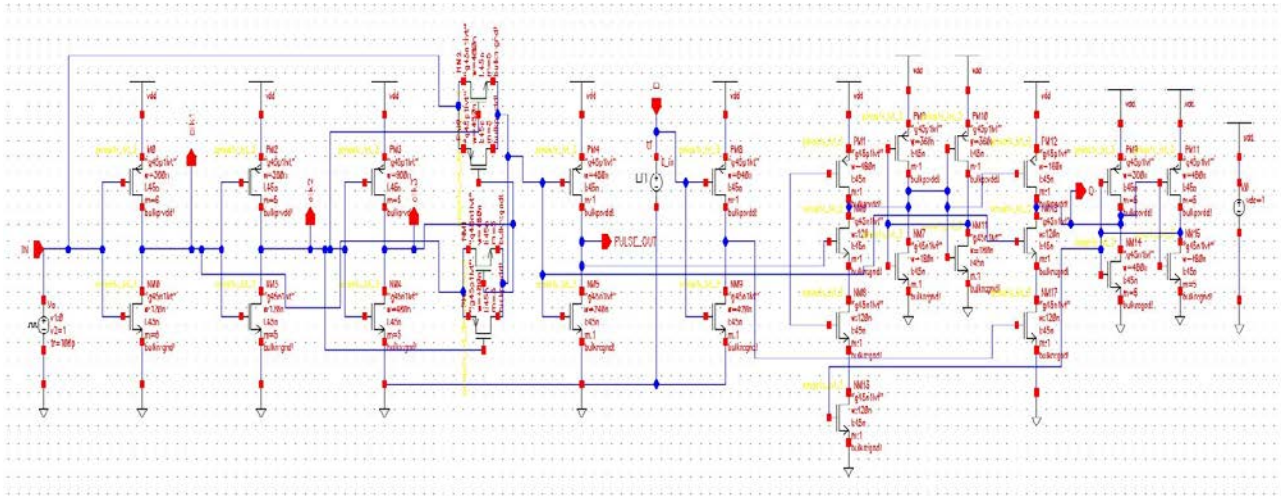

Fig. 3. Schematic Capture of SCDFF

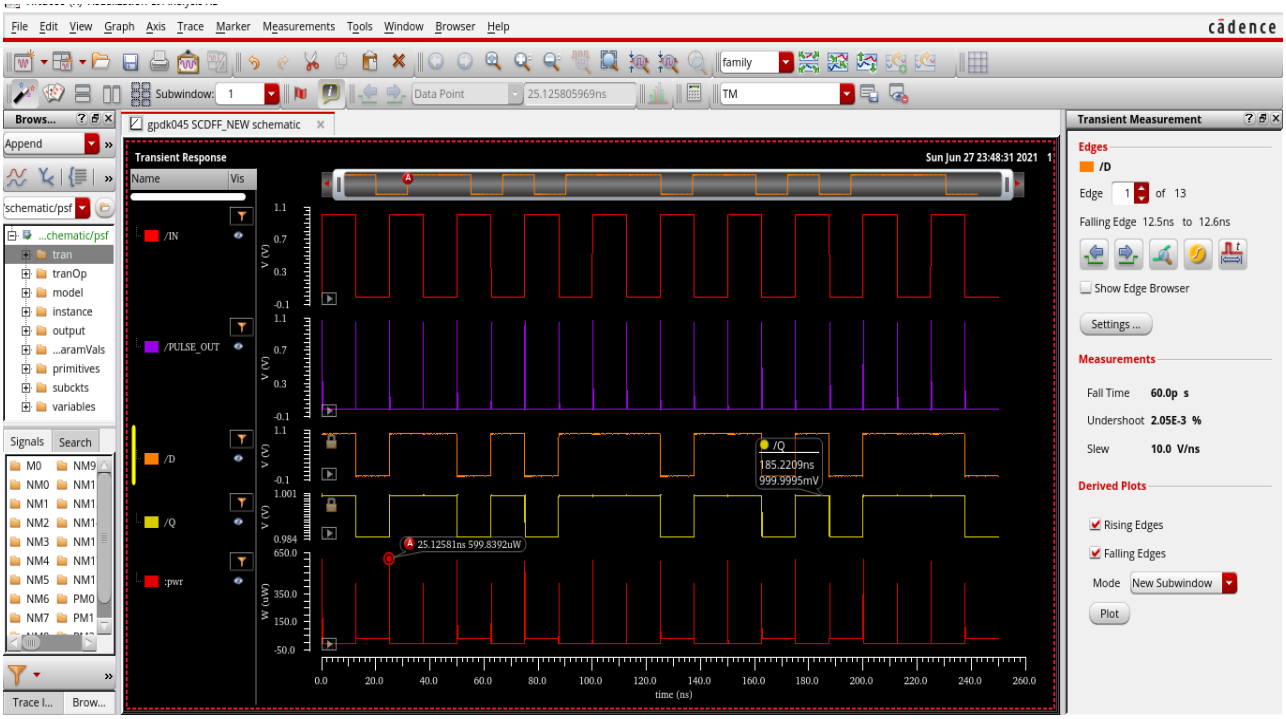

Fig. 4. Analog Simulation Implementation of SCDFF

The above simulation results shown in Fig. 5, the latch is following its inputs which depict the functionality of the FF. In general, the flip-flops capture either at positive or negative edge of the flip-flop. This dual edge triggered captures the data at both positive edges and negative edges of the clock.

The output waveform in the above simulated result presents the power consumed by the design, it was captured peak power as approximately 600µW.

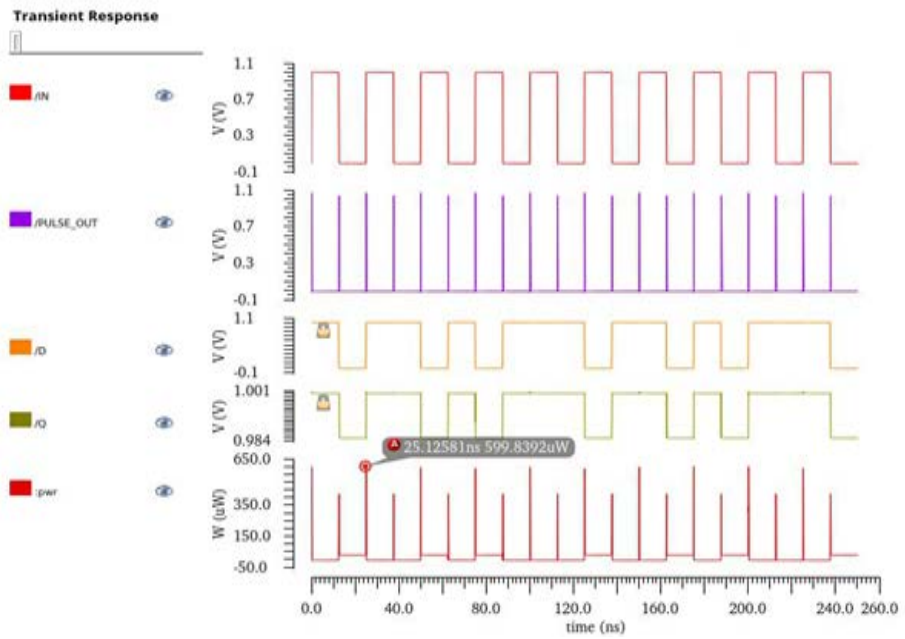

Fig. 5. Transient.Response.of. SCDFF

4. Dual Edge Triggered Static Pulsed Flip-flop

Fig. 6 shows the Pulse Generator for DETSFF, this delivers pulses at each of the positive edges and negative edges of the input clock CLK.

Fig. 7 is a 6T SRAM cell with two inverters to capture Q and Qbar (QB) operates with the pulses generated at every edge of clock in pulse generator circuit. This circuit is design targeting a 45nm technology library.

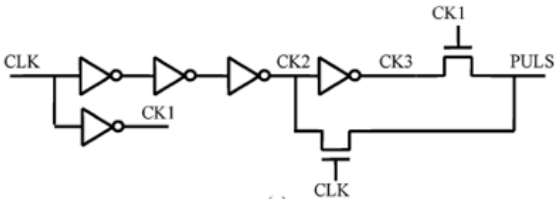

Fig.6. A Pulse Generator

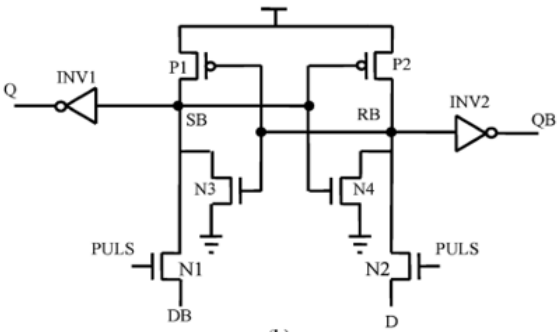

Fig. 7. 6T SRAM cell

To initiate delayed versions of clocks, a chain of four inverters is employed in the pulse generator. By the aid of two pass transistors, delayed versions of the clock are employed to form sample windows around the rising edges and falling edges of clock. The inputs to the latch, are supplied directly to the SB lines and RB lines via pass transistors that are controlled by a pulse signal Because the inputs are fed directly, a slight delay can be obtained. To keep the SB and RB nodes from floating, pMOS transistors P1, P2 and N1, N2 weak nMOS transistors are utilised. Despite the fact that the static nature of DSPFF prevents needless transitions, lowering power consumption in the circuit, DSPFF utilizes a lot of power due to the significant leakage current. Because of the enormous capacitive load at the SB and RB nodes, latency is degraded. By altering the aspect ratio of transistors, symmetrical output delays can be achieved. Because the gate drive voltage (Vdd - Vthn) for SB and RB nodes cannot be exceeded, there could be distortion in Q and QB at low working voltages.

4.1. Implementation of DETSPFF

A test bench is created to simulate the above design, the test bench carries a clock operates at 50ns and data input D is generated at the similar frequency of the clock to eliminate the Setup and Hold time violations of the latch. The transient analysis is carried out with the following parameters. Transient Analysis parameters: Stop time: 250ns (D input pattern repeated for two times) V_{bias}: 0.2V.

4.2. Schematic of DETSPFF

Fig. 8 shows the schematic design of DETSPFF which is implemented using above Transient analysis parameters. Fig. 9 shows the Analog simulation implementation of DETSPFF using Cadence. The below simulation results shown in Fig. 10, the latch is following its inputs which depicts the functionality of the FF. In general, the flip-flops captures either at positive edge or negative edge of the flip-flop. This DET captures the data at both edges of the clock.

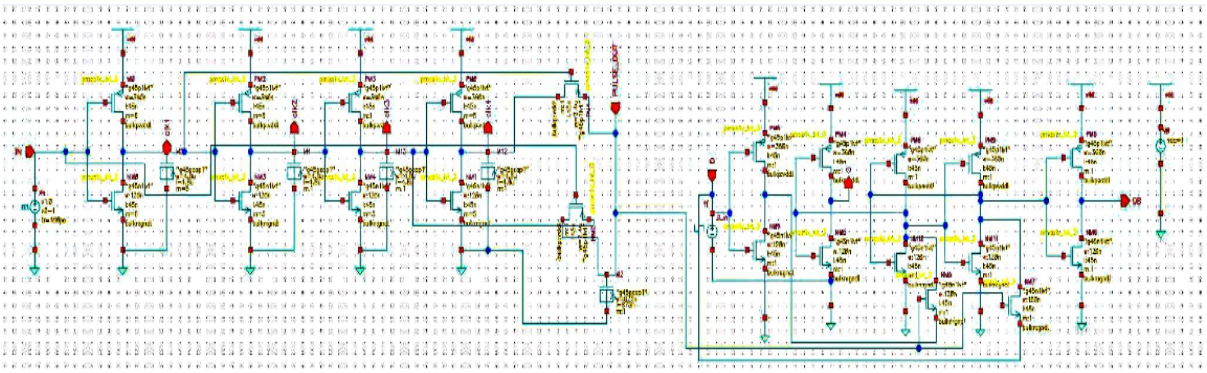

Fig. 8. Schematic Capture of DETSPFF

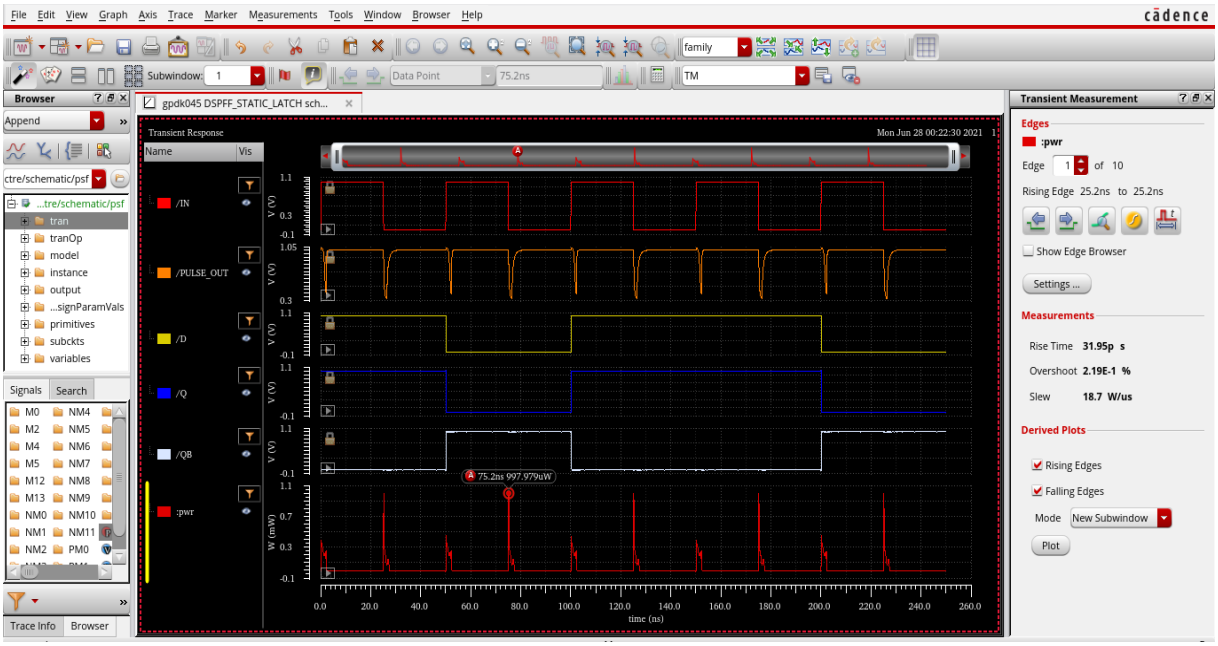

Fig. 9. Analog Simulation Implementation of DETSFF

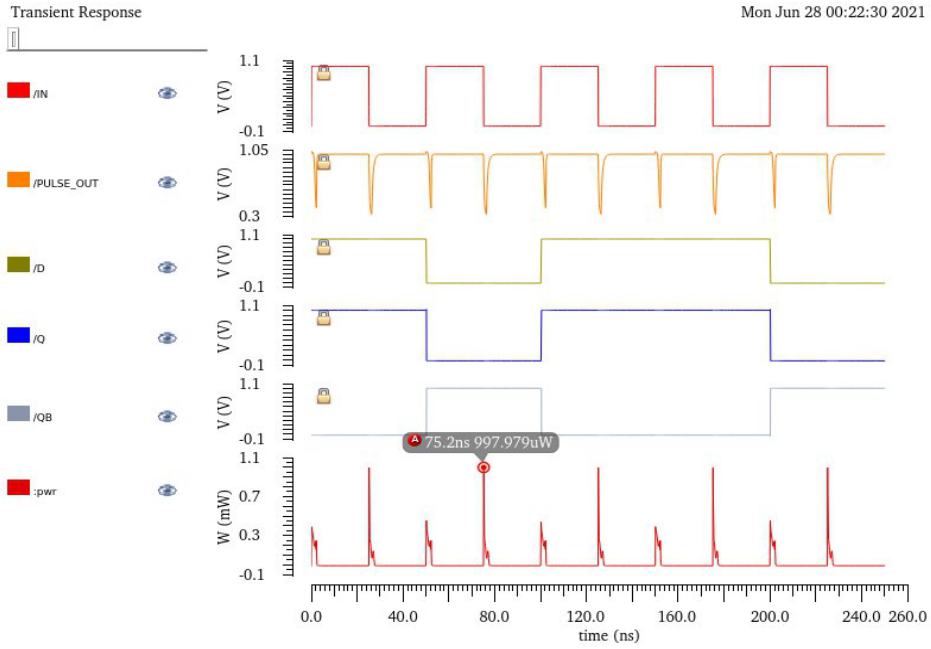

Fig. 10. Transient Response of DETSFF

The waveform in the above simulated result, the power consumed by the circuit and it was captured peak power as approximately 997µW shown in Fig.10. The above waveform shows the power of the implemented design as shown in respective circuits. The power has even increased when compared to previous circuit.

5. Previous Work on Dual Edge Triggered Flip-flop [6]

The pulse generator shown in Fig. 11 sets-up short pulses at the rising edge of the input clock and falling edge of the input clock CLK.

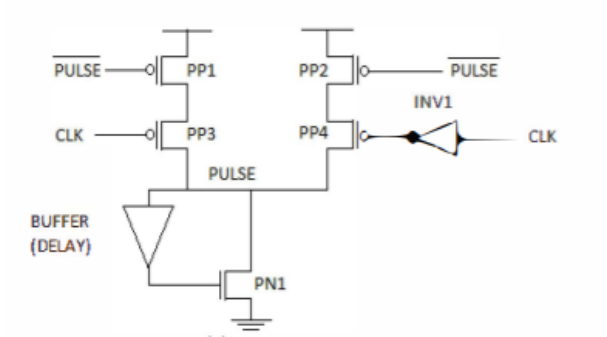

Fig. 11. Pulse Generator

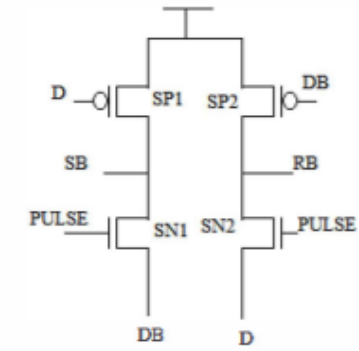

Fig.12.Sense Amplifier

Fig. 12 represents a sense amplifier which generates SB and RB signals based on the pulse generated by the pulse generator.

Fig. 13 is the SAFF is an added fast FF with a near-zero or negative setup time. The SAFF is added with a SA stage and a slave latch The SA stage might occupy data just exactly for the positive edge of clock, and the output of the SA stage could be preserved during the positive half cycle of clock. Thus, the sizing difficulty in the pulse-based flip-flop (PFF) is detached. For a near-zero or negative setup time and a reduced hold time, the SAFF is an excellent design for substitute Master slave flip-flop (MSFF), which is the standard cell library for high-speed design. However these features are very attractive, the SAFF has numerous issues.

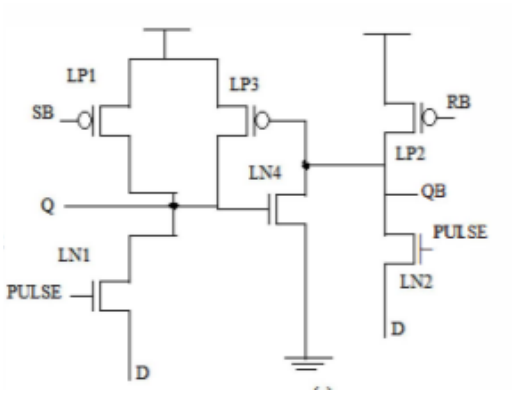

Fig. 13. Sense Amplifier based Flip-flop

5.1 Schematic of Previous Work on DETFF [6]

Fig. 14 shows the schematic design of Previous Work on DETFF which is implemented using above Transient analysis parameters. Fig. 15 shows Analog simulation implementation of DETFF using cadence.

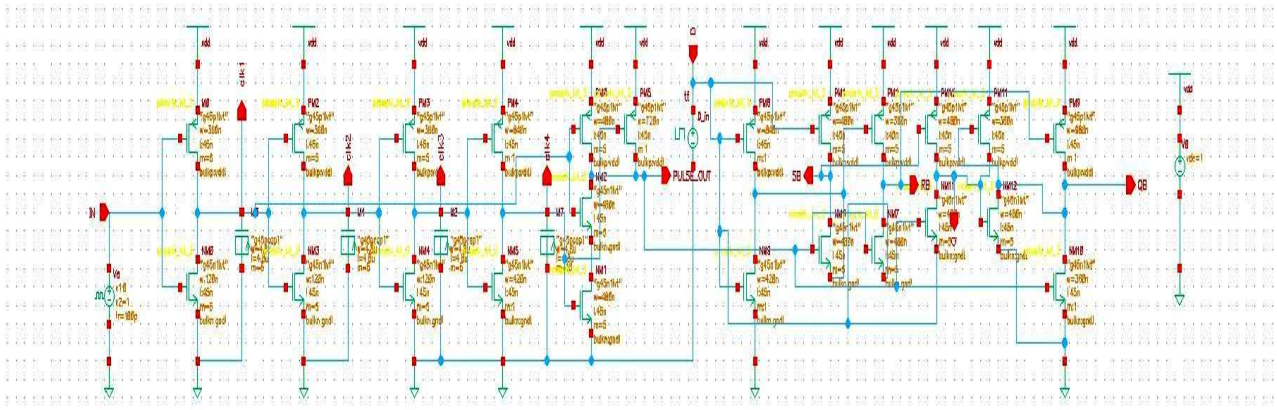

Fig. 14. Schematic capture of Previous Work on DETFF

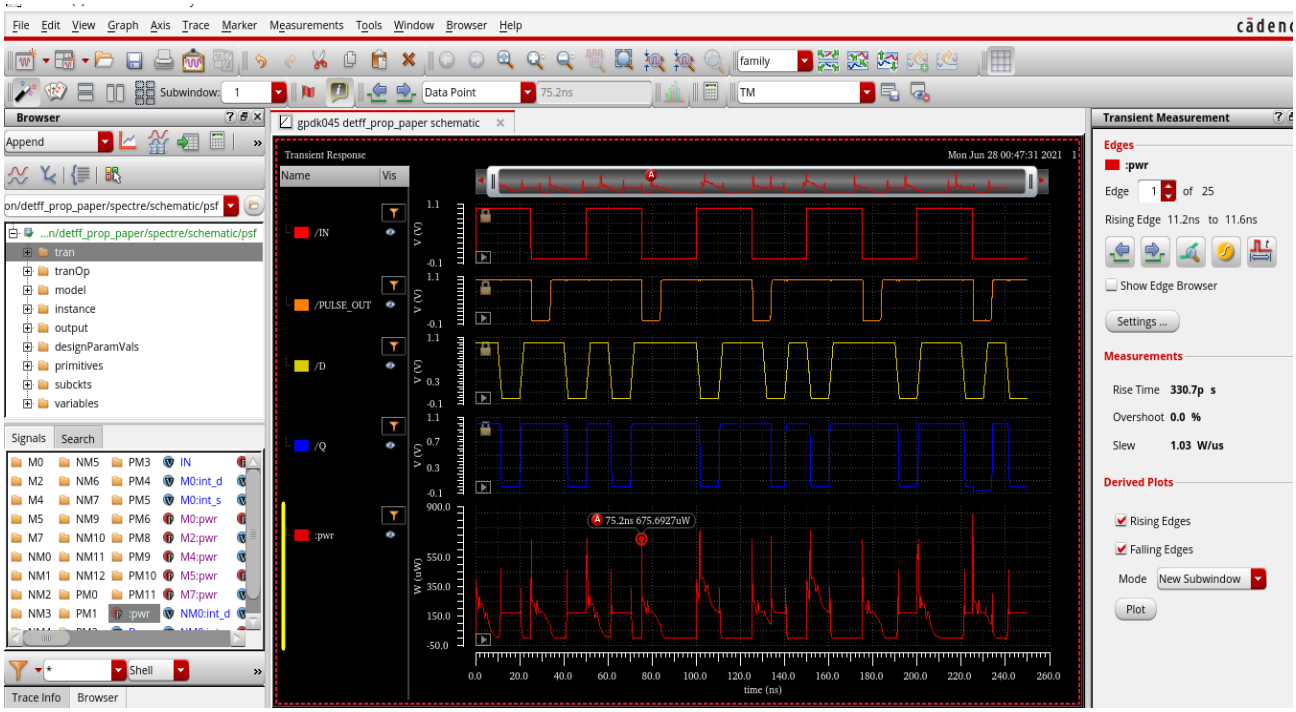

Fig. 15. Analog simulation with Spectre of Previous Work on DETFF

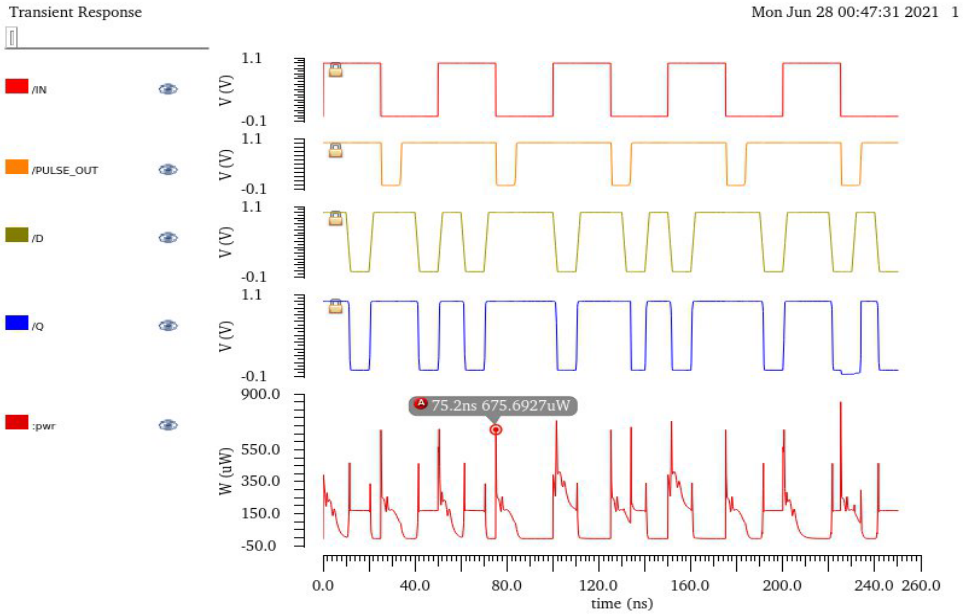

Fig. 16. Transient response of the Previous Work on DETFF

The whole design is simulated using “Cadence Tool”. The Static Output Controlled Discharge Flip-flop (SCDFF) and Dual Edge Triggered Static Pulse Flip- flop (DETSFF) are the designs which are not much useful when it comes to the parameters like area and power consumption. The SCDFF has many transistors and the DETSPFF consumes more power. So the previous work on DETFF design is more feasible when compared to previous two designs in both the parameters. The last waveform in the above simulated result illustrate the power consumed for the above circuit and it was captured peak power as approximately 675µw as shown in Fig. 16.

6. New Proposed Low Power Dual Edge Triggered Flip-flop with High Speed Enhancement

This circuit is design targeting a 45nm technology library. The circuit is fine-tuned and defined the aspective ratio of each transistor in all the blocks.

Fig. 17 illustrates an EXOR gate-based pulse generator. That creates brief pulses at the input clock CLK's falling and rising edges. Fig. 18 shows a low power dual edge triggered flip flop that makes the advantage of the pulse generator's pulse. This flop records data at both the clock's edges.

This design has two stages, one is a pulse generator and the second stage.is a latching stage. The pulse generates a narrow pulse as PULS and the same is connected to the latching stage as PLUS and PLUSB. When PLUS is low the latch holds the previous value and captures the data when PLUS is high. As these PLUS signals are short pulses generated at either end of rise and fall edges of the clock, this latch captures the data at both the edges making it dual edge triggered. This captures the data at double rate and hence its faster compared to normal flip-flops.

When a pulse occurs during the latching step, D and DB can assist Q and QB in the charging and discharging immediately. This significantly decreases the clock to Q delay and improves the circuit's-speed performance. The circuit's efficiency is determined by the pulse width. The circuit is developed and fine-tuned to keep the pulse width as small as possible for optimum power savings.

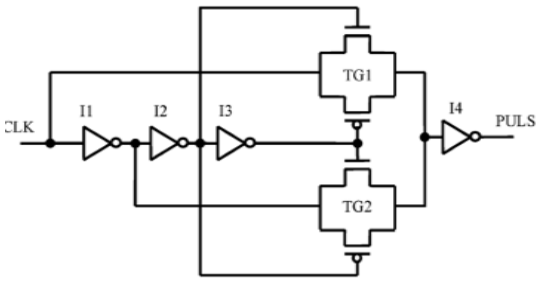

Fig. 17. Exor Gate-based Pulse Generator

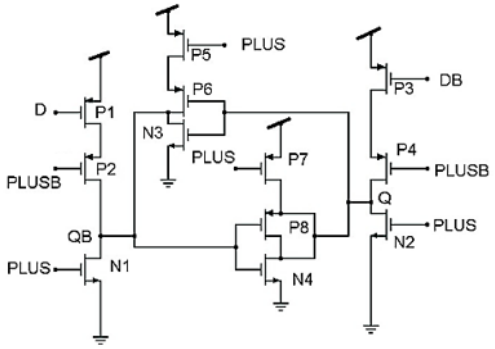

Fig. 18. Low power Dualedge triggered flip flop.

Newly proposed Low power dual edge triggered flip-flop circuit is fine tuned to get optimization in this design with respect to pulse generator and latch. Here, in this design the density of the transistors is increased when compared to the previous designs. The clock will generate short pulses at both the edges of the clock. The main key factor in this design is optimizing the pulse generator to produce short pulses. The functionality is that each and every pulse generated is capturing the data and producing the results.

6.1. Schematic of New Proposed Dual Edge Triggered Flip-flop with High Speed Enhancement

Fig. 19 shows the schematic design of new proposed DET static pulsed flip-flop which is implemented using above Transient analysis parameters. Fig. 20 shows analog simulation implementation of new proposed DET static pulsed flip-flop in cadence.

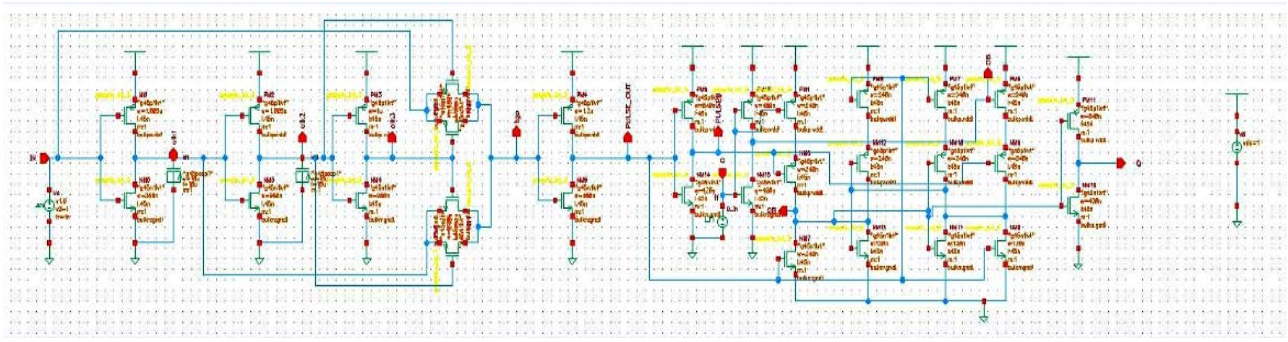

Fig. 19. Schematic Capture of New Proposed low power DETFF

Fig.20. Analog simulation with spectre of New Proposed low power DETFF

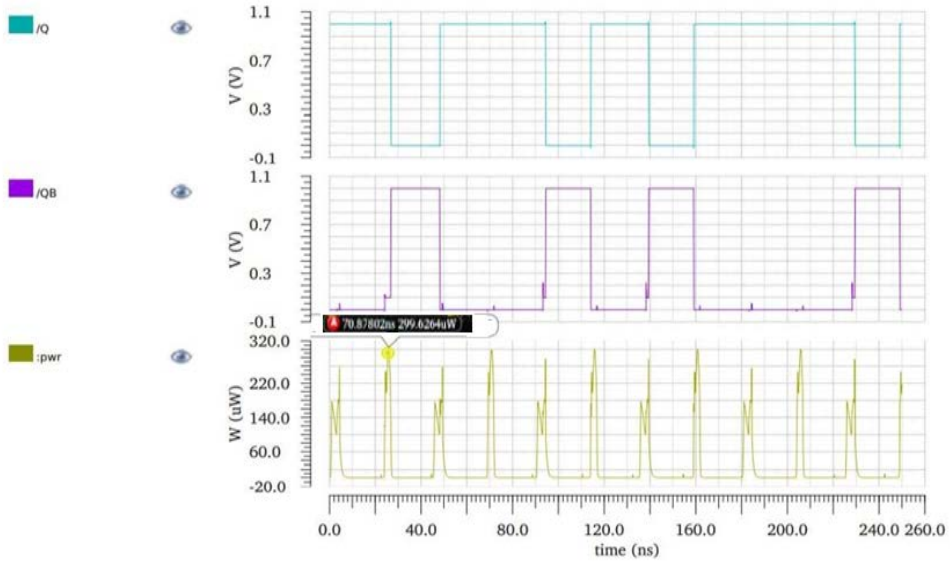

Fig. 21. Transient response of the New Proposed low power DETFF

The following simulation results shown in Fig. 21, illustrate the latch is following its inputs which depicts the functionality of the flip-flop. In general, the FF captures either at positive or negative edge of the flip-flop. This dual edge triggered captures the data at both edges of the clock.

The last waveform in the above simulated result shows the power consumed by the circuit and it was captured peak power as approximately 299μW.

The results prove power consumption which is drastically reduced compared to the circuits which are previously implemented. Approximately half of the power is reduced making the circuit to operate with high speed for the new proposed low power DETFF.

7. Simulation Parameters and Results

The proposed DETFF has the other advantages as following:

(1) Results in a latch sufficiently immune from glitches,
(2) Allows for the strong passage of data signals using single pass transistor of the same transistor type,
(3) Sufficiently reduces contention in the hold portion,
(4) Because of the reduction in the number of devices, the wiring necessary for the clock line of this latch is reduced. The proposed DETFF is simple in design, robust and reliable in operation, and efficient in operation.

Table 1 indicates the Simulation parameters which are used when designing the circuit.
The technology used here is 45nm with min and max width as 120nm and 360nm respectively.

Table 1. Simulation Parameters

SIMULATION PARAMETERS	
Technology	45nm
Min Width	120nm
Max Width	360nm
Library	Fast1vddo_hvt
Power	Vdd = 1V
Duty Cycle	50%
Clock Frequency	50MHz

Table 2 shows the comparison results of the flip-flops taken in the paper.

Table 2. A Comparison Table Results

Design Name	Total Average Power (μW)	Time Delay (ns)
SCDFF	600	25.12
DETSPFF	997	75.25
Previous work on DETFF[6]	625	75.18
New Proposed Low Power DETFF	299	70.87

From the table 2, observation of the above results in terms of Power (in μW) and Time delay (in ns), it is clear that

1. The SCDFF consumes 600 μW with 25.12ns delay.
2. DETSPFF dissipates more power compared to Static Output-Controlled DETFF i.e., DETSFF i.e., 997 micro Watts with 75.25 ns.
3. The previous work on DETFF [6] consumes 625μW with 75.18ns time delay.
4. The last circuit, which is newly proposed low power DETFF. It dissipates very minimum power when compared to previous circuits as shown in the table. There is a drastic decrease in power i.e., it consumed only 299μW with 70.87ns time delay. Here time delay plays an important role for the Speed Enhancement.

7.1. Merits

1. For the half of the clock frequency, DET offers the same throughput.
2. Because of the reduction in the number of devices, the wiring necessary for the clock line of this latch is reduced.
3. Results in a latch sufficiently immune from glitches.

8. Conclusion

It has been observed that a significant amount of power consumption is generated by the clock line. The proposed design were the signal feed-through from input source to the internal node of the latch, shorten the transition time and enhance trade-off between both the power and speed performance. This paper compares four previously published DETFFs together with our design for different metrics. As compared to three previously published DETFFs, the design of new proposed low Power DETFF out performs in terms of power consumption and power- delay-product. Especially, the proposed flip-flop is superior in power reduction at different parameters, hence, proves better suited for low-power digital system applications.

The SCDFF consumes 600 μW with 25.12ns delay. DETSPFF dissipates more power compared to Static Output-Controlled DETFF i.e., DETSFF i.e., 997 micro Watts with 75.25 ns. The previous work on DETFF consumes 625μW with 75.18ns time delay. The last circuit, which is newly proposed low power DETFF, It dissipates very minimum power when compared to previous circuits. There is a drastic decrease in power i.e., it consumed only 299μW with 70.87ns time delay. Here time delay plays an important role for the Speed Enhancement.

Acknowledgment

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