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A Review of NBTI Degradation and its Impact on the Performance of SRAM

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***Abstract*—**Temporal degradation of VLSI design is a major reliability concern for highly scaled silicon IC technology. Negative Bias Temperature Instability (NBTI) in particular is a serious threat affecting the performance of both digital and analog circuits with time. This paper presents a review of NBTI degradation, its mechanism and various factors that affect the degradation caused by NBTI. Reaction Diffusion (RD) model based analytical expressions developed by various researchers are also discussed along with their features and underlying assumptions. Degradation in the Static RAM (SRAM) performance caused by NBTI is also discussed in detail along with the strategies that are employed to combat the effect of NBTI degradation in SRAM. Results of the review done for SRAM cell under NBTI degradation suggests that these design strategies are effective in improving the SRAM cell performance.

***Index Terms*—**NBTI, Positive Bias Temperature Instability (PBTI), Static Noise Margin (SNM), Hot Carrier Injection (HCI), Reliability, Threshold Voltage, RD model, SRAM, Genetic Algorithm (GA), Body Bias (BB), Yield.

I. Introduction

Bias Temperature Stability (BTI) is a serious threat in scaled CMOS technology which affects the performance of VLSI circuit with time. Negative Bias Temperature Instability (NBTI) is a reliability concern that is associated with PMOS transistor and it affects the performance parameters like threshold voltage, transconductance, saturation current etc. [1]. Similar to NBTI effect in PMOS transistors, NMOS devices suffer from Positive Bias Temperature Instability (PBTI) but its affects on the performance of VLSI chip are not much severe as compared to NBTI particularly in case of SiO_2 dielectrics. The use of high K dielectric stacks started to be employed from 32nm technology has increased the overall ageing degradation [22]. Apart from NBTI and PBTI other sources of reliability degradation includes Hot Carrier Injection (HCI), Time Dependent Dielectric Breakdown (TDDB), Radiation induced damage etc. [2]. These sources of reliability degradation can cause severe performance issues in NMOS and PMOS devices and can drastically reduce the functional yield. NBTI occurs in negatively biased PMOSFETs at elevated temperature and is a consequence of interface trap generation at Si/SiO_2 interface [8]. One of the important features of NBTI is recovery i.e. when stress is removed the degradation in threshold voltage (v_{th}) is recovered to a certain extent but the degradation in vth caused due to channel hot carriers (CHC) cannot be recovered [9].

Digital circuits are more likely to suffer NBTI effects [26] but the effect of NBTI on SRAM is more significant as compared to that in the random logic circuits [20]. The degradation in Read Static Noise Margin (RSNM) that is caused due to NBTI degradation can cause memory failure. Research work carried out in [2, 19, 20, 21, 22] deals with NBTI degradation effects on SRAM and its important performance parameters. Design techniques employed to mitigate the NBTI degradation effects are discussed in [19, 20, 22, 24, 33].

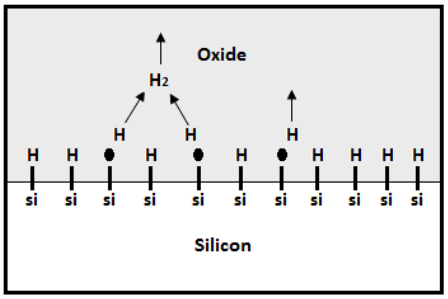
The rest of the paper is organized as follows: Section II deals with the mechanism of NBTI degradation, RD model of NBTI degradation is explained in section III. Section IV highlights important cognizance on NBTI, Section V investigates the effect of NBTI degradation on the performance of 6T SRAM cell. Strategies for mitigating the performance degradation caused due to NBTI in 6T SRAM cell are described in Section VI and finally in Section VII conclusions are drawn.

II. NBTI Degradation Mechanism

NBTI (Negative Bias Temperature Instability) is one of the most important reliability concerns in nanoscale PMOS devices. This occurs in PMOS devices when they are subjected to negative gate voltage with respect to source and drain terminals i.e. when $v_{gs} = -v_{dd}$ and drain to source voltage v_{ds} is kept at 0 volts. The PMOS device under this condition works in strong inversion and this causes an increase in the absolute value of the device threshold voltage (v_{th}) over time. PMOS device under this condition is said to be stressed and if continues to be in stressed state for a longer period of time then the threshold voltage shift can cause serious threat to the overall functionality of the VLSI chip. The term negative

bias comes from the fact that gate voltage is made negative with respect to the source and drain terminals and since the degradation phenomena is strongly dependent on temperature that is the reason why temperature instability term is used in NBTI. Aggressive scaling of the device dimensions in particular the gate oxide thickness has brought the poly silicon gate closer to Si/SiO_2 interface [1] and this has enhanced the NBTI degradation in PMOS devices because of the increased value of electric field.

During fabrication, hydrogen passivation is done right after the oxidation process so as to remove the dangling Si atoms. In stress phase and at elevated temperature these weak Si-H bonds can be easily broken and this leads to the generation of donor like state known as interfacial traps which is regarded as a prime contributor to the increase in the device threshold voltage over time. Neutral H atom is a slow diffuser but two H atoms can combine to form a H_2 molecule which diffuses relatively faster in the oxide than H atom. So NBTI is a result of continuous trap generation in Si/SiO_2 interface of PMOS transistor [2]. Some literature also suggests that during NBTI stress, the number of interface traps becomes equal to the positive charges in the oxide bulk [3, 4]. Fig. 1 shows NBTI mechanism in PMOS transistor where it is clearly shown that the diffusing species can be an H atom or H_2 molecule.



$$si3 \equiv siH + H^+ \leftrightarrow si3 \equiv si\bullet + H_2$$

Fig.1. Schematic of interface trap generation ($si\bullet$) and H/H_2 species diffusion during NBTI stress

NBTI degradation results in increasing the absolute value of the threshold voltage of the PMOS device which in turn leads to the reduction in the drain current, transconductance and mobility. It has been observed that the effect of NBTI becomes more severe because of the introduction of nitrogen into the gate dielectric which is done primarily to reduce the boron penetration from P+ poly gate into the thin oxide and also for reducing the gate leakage [5]. Criterion for the device failure is still a debatable topic, Schroder et al. [6] proposed that device failure criteria is often benchmarked at v_{th} shift of 50 mV or $\Delta I_{ds}/I_{ds}$ ~ 10% but still it is circuit dependent.

III. Overview of Reaction Diffusion (RD) Model

Reaction Diffusion framework based model of NBTI degradation is one of the most widely used model for predicting the NBTI induced threshold voltage degradation in PMOS device. Mahapatra et al. [1] proposed a model for estimating the v_{th} degradation due to NBTI based on the assumption that the oxide thickness (t_{ox}) is infinite and poly silicon acting as a reflector or absorber. Model proposed in [1] considered H as the dominant diffusion species; however the debate regarding the nature of the diffusion species continued for a long time and depending on this fact the estimated degradation in the performance of PMOS device has varied significantly. Recent experiments have indicated that H_2 is a dominant diffusion species instead of H [7]. Hadlun et al. [8] proposed RD framework based model for predicting the number of interface traps generated under three different situations. One is when H is the diffusion species, second is when H_2 is the diffusion species and third case considers both H and H_2 as the diffusion species. Considering H as the diffusion species [8], the rate of generation of interfacial traps is given by-

$$\frac{dN_{IT}}{dt} = K_F[N_0 - N_{IT}] - K_R N_{IT} N_H \quad (1)$$

Where K_F is the forward reaction rate (Si-H bond breaking rate), K_R is the reverse reaction rate (Si-H bond annealing rate). N_0 is the initial concentration of Si-H bonds i.e. Si-H bond density at Si/SiO_2 interface. N_H is the concentration of hydrogen at the Si/SiO_2 interface.

$$\frac{dN_H}{dt} = D_H \frac{d^2 N_H}{dx^2} \quad (2)$$

Interfacial trap generation leads to the generation of H atoms which diffuse away from the Si/SiO_2 interface towards the gate terminal. Diffusion of H atoms follows the following equation-
where D_H is the diffusion constant for hydrogen.

Solution of equation (1) and (2) yields-

$$N_{IT}(t) = \sqrt{\frac{K_F N_0}{2K_R}} (D_H t)^{1/4} \quad (3)$$

$$\Rightarrow N_{IT} \propto t^{1/4}$$

So, for H only diffusion, the value of time exponent (n) is 0.25. H atoms released as a result of Si-H bond dissociation reacts to form H_2 molecule which diffuses away towards the gate terminal.

$$H + H \leftrightarrow H_2 \quad (4)$$

As discussed in [8] the interfacial traps density in case of H_2 only diffusion is given by-

$$N_{IT}(t) \propto \left[\frac{K_F N_0}{K_R}\right]^{\frac{2}{3}} (D_{H_2} t)^{\frac{1}{6}} \quad (5)$$

where D_{H2} is the diffusion constant for H_2 molecule. This equation shows that interfacial trap density varies with time as-

$$N_{IT} \propto t^{1/6} \tag{6}$$

with time exponent of (n = 1/6).

Authors in [8] does not include the dependence of K_F on the number of holes (p), their ability to tunnel to the Si-H bonds (T_{COEFF}), capture cross section of the Si-H bond (σ_o) and any field dependence of Si-H bond dissociation (B). These dependencies are very well addressed in [1] so as to accurately predict the NBTI degradation effects on a PMOS device. Wenping Wang et al. [9] considered parameter p in the RD model and suggested that the generation rate of interfacial trap is governed by the following equation-

$$\frac{dN_{IT}}{dt} = K_F[N_0 - N_{IT}]p - K_R N_{IT} N_H \tag{7}$$

The density of holes as suggested in [1,9] is given by

$$p = c_{ox}(vgs - vth) \sim E_{ox} \tag{8}$$

where E_{ox} is the oxide electric field. Predictive model for NBTI degradation based on RD framework in case of static NBTI is proposed in [7,10]. These models are also accurate in terms of predicting v_{th} degradation due to NBTI and the simulation results obtained using these models match the experimental data. However these models do not incorporate the fact that there will be a fractional drop in the concentration of hydrogen at Si/poly interface. This model is incorporated in the model proposed in [9]. Vattikonda et al. [10] suggested that non H based mechanisms may have faster response time than the diffusion process and the same is incorporated in the model proposed in [10] by including a constant δ (5 mV) in the stress and recovery equations. The threshold voltage degradation due to NBTI can be estimated using-

$$\Delta v_{th} = \left(\frac{qN_{IT}}{c_{ox}}\right) \tag{9}$$

Trap generation at the interface also leads to the scattering which results in mobility degradation. Krishnan et al. [11] suggested that the decrease in the mobility results in additional v_{th} shift and this effective v_{th} shift considering mobility degradation [12] can be expressed as-

$$\Delta v_{th} = \left(\frac{qN_{IT}}{c_{ox}}\right)(1+m) \tag{10}$$

Constant m is a technology specific parameter and it represents the equivalent v_{th} shift which occurs due to degradation in the mobility. Bharadwaj et al. [7] proposed a relation for estimating the long term v_{th} degradation (LTD) considering its dependence on the duty cycle and frequency of operation. Dependence on duty cycle (α) and frequency ($1/T_{clk}$) is given by-

$$\Delta v_{th}(LTD) = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1-\beta_t^{1/2n}}\right)^{2n} \tag{11}$$

Where-

$$\beta_t = 1 - \frac{2\xi_1 t_e + \sqrt{\zeta_2 C(1-\alpha)T_{clk}}}{2t_{ox} + \sqrt{Ct}}$$

$$C = \frac{1}{T_o}\exp\left(-E_a/KT\right)$$

$$K_v = \left(\frac{qt_{ox}}{\varepsilon_{ox}}\right)^3 K^2 C_{ox}(V_{gs} - V_{th})\sqrt{C}\exp\left(\frac{2E_{ox}}{E_o}\right)$$

Where t_{ox} is the oxide thickness, t_e is the effective oxide thickness, ξ_1 , ξ_2 & E_o are constants, E_a is the activation energy, C_{ox} is gate oxide capacitance per unit area.

IV. Important Cognizance on NBTI

1. Dynamic NBTI degradation occurs under AC operation and results in less v_{th} shift of PMOS as compared to DC stress operation [1, 2, 13, 17]. Device life time increases under ac stress condition and the prime reason for this fact is that during AC operation there will be recovery cycles during which hydrogen atoms diffuses back and reacts with the dangling silicon atoms to form Si-H bonds thereby reducing the number of available interfacial traps. Fig. 2 shows stress and recovery phase of NBTI indicating that during relaxation there occurs recovery in V_T shift to a certain extent.

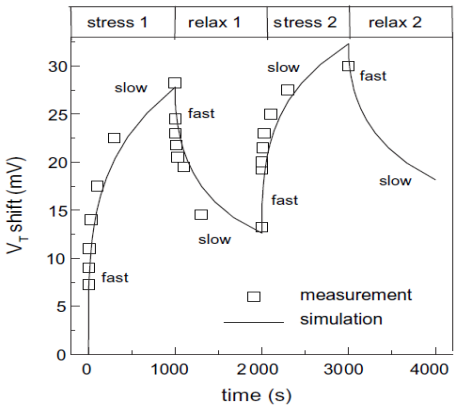


Fig.2. Stress and relaxation phases of NBTI showing recovery during relaxation phase [1].

2. High K dielectric like HfO_2 is a candidate for replacing SiO_2 and several metals such as W, Re, TiN & TaN are under exploration to replace the polysilicon gate [13]. Experimental data shows that high K metal gate PFETs have similar NBTI effect as that of the conventional oxide/poly PFETs at elevated temperature.
3. Basic RD model predicts no frequency dependence of NBTI degradation [15]. NBTI degradation is significantly reduced at higher frequencies. Frequency dependence can be described by taking a reference frequency fo ∈ [1KHz, 1MHz] according to-

$$V_T(f) = V_T(f_O)\left(\frac{f}{f_O}\right)^{-0.03323}$$

4. Nitrogen, water and hydrogen in the oxide degrade the NBTI degradation [18]. It is a point to note that hole trapping into the pre-existing oxide defects is negligible for properly processed gate oxide films [23].
5. Trap generation/passivation is strongly affected by the boundary conditions at the oxide/poly-si boundary [16]. Initial value of the interface traps may significantly affect the power index n which is derived using RD model in diffusion limited region.
6. NBTI is still a concern even for the multigate FETs (FINFETs) and this is because of the increasing number of dangling Si-H bonds that are available at Si/SiO_2 interface [28].
7. Threshold voltage shift due to NBTI degradation is strongly dependent on the doping concentration of the substrate, effective oxide thickness (EOT), stress voltage and temperature [14].

V. 6T SRAM Cell under NBTI Degradation

A conventional 6T SRAM cell consists of two cross coupled inverters and two access transistors that provides the access of the internal storage nodes to bit line and bit bar line. Fig. 3 shows schematic diagram of 6T SRAM cell under NBTI degradation. One of the PMOS transistors in 6T SRAM cell will always have a '0' input at its gate terminal. Suppose that internal node Q is storing logic '0' and Qbar is storing a logic '1' then

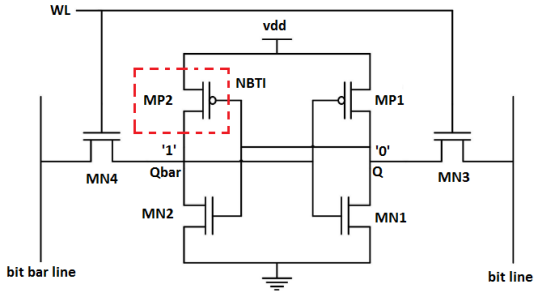


Fig.3. 6T SRAM cell under NBTI degradation.

the PMOS transistor MP2 will undergo NBTI degradation because its gate to source voltage is negative ($-v_{dd}$ volts) and drain to source voltage is 0 volts which is a required condition for NBTI degradation.

The change in the threshold voltage of MP2 can lead to performance degradation of 6T SRAM cell thereby affecting its various important performance parameters like SNM, read delay, write delay. SNM quantifies the amount of voltage noise required at the internal nodes of a bit cell to flip the cells content [30]. Seevinck et al. [31] proposed a graphical technique for the estimation of SNM of SRAM cell. SNM can be obtained by drawing and mirroring the inverter characteristics and finding the maximum possible square b/w them [31]. Kang et al. [2] and Kumar et al. [19] have analyzed the performance degradation in SRAM cell and found that RSNM of the cell decreases under NBTI degradation. RSNM shows a decline of more than 10% from its original value in 3 years time duration (10^8 sec), however the effect on hold SNM is not very severe and the same is found to be degraded by less than 0.3% in the same time duration [2].

The prime reason for the reduction in the RSNM value can be understood as follows: NBTI in transistor MP2 will cause an increase in its threshold voltage. During read operation WL='1' and bilt line and bit bar line are precharged to v_{dd} volts. MN3 and MN4 transistors are turned on and the voltage at node Q will start to increase, increased threshold voltage of MP2 will cause it to turn off earlier before MN2 starts conducting and as a result the voltage at node Qbar will start to decrease and a condition will arise where strong coupling of the inverters will cause the stored data bits to flip. As a result of NBTI one of the VTCs of 6T SRAM cell moves horizontally thereby making the lobe of butterfly curve smaller, resulting in reduced RSNM.

Kim et al. [22] analyzed the impact of NBTI on V_{min} (minimum voltage of operation) for SRAM cell. V_{min} is a major design concern for optimizing the SRAM circuit in terms of power and energy. V_{min} is determined by the performance requirement rather than the stability requirement [22]. It was observed that NBTI has a strong impact on the value of SNM limited V_{min}, this is because of stronger pull down transistor as compared to pull up transistor which causes the trip point of inverter to shift at a lower voltage level. Degradation of around 180mV in SNM limited V_{min} is observed over the period of stress at 32nm technology node. Similar results on Data Retention Voltage (DRV) are presented in [7] where it is found that there occurs around 12% increase in DRV in a time span of 5 years.

Another important parameter that suffers due to NBTI degradation is read delay. Read delay is defined as the time delay between 50% level change of the word line signal to 50 % level change of the output of the sense amplifier. According to observations highlighted in [7, 9, 22] on read delay it can be predicted that read delay of 6T SRAM cell under NBTI does not degrade much. This is because read delay is estimated by the pull down current path which is formed by access transistor and the pull down transistors. Since both the access transistor and pull

down transistors are made up of NMOS transistor so it is obvious that NBTI will not cause any major change in the read delay of 6T SRAM cell.

Authors in [7,19] have found that there occurs a reduction in the write delay in both 1-0 and 0-1 transitions during data write operation. This is because of the weakening of the PMOS pull up transistor which is affected by NBTI and this supports the bit flipping during data write operation.

Hold margin also shows a degradation of around 5% in a time span of 5 years [7]. Fig.4 shows the variation of various important performance parameters: DRV, hold margin, read margin, write delay and read delay with time at 90nm technology node.

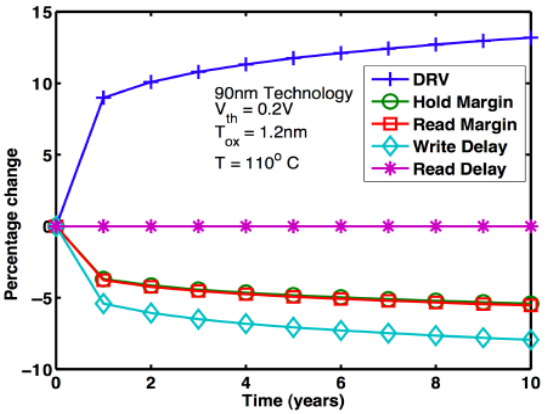


Fig.4. Change in the values of SRAM performance metrics with time [7].

Kang et al. [2] analyzed the effect of NBTI degradation on read failure and write failure probability of 6T SRAM cell. Read failure occurs if the data stored in an SRAM cell flips while reading the cell [32]. On the other hand, write failure occurs if cell data cannot be flipped while writing [32]. Authors in [2] have used Critical Point Sampling (CPS) method for computing the read failure probability. Overall read failure probability is calculated using the following equation:

$$P_{RF}(t) = P_{RF,H} S_H + P_{RF,L} S_L$$

Where S_L & S_H are the signal probability of the cell state being low and high respectively. $P_{RF,L}$ is the read failure probability for the low state and $P_{RF,H}$ is the read failure probability in high state. Read failure probability for different signal probability values is plotted in Fig.5. It can be observed from Fig.5 that P_{RF} increases when signal probability values are unbalanced. S_L=1% indicates the most unbalanced condition of signal probability that is taken into consideration and read failure probability in this case increase by 2.9 times as compared to the case when S_L value is 50%.

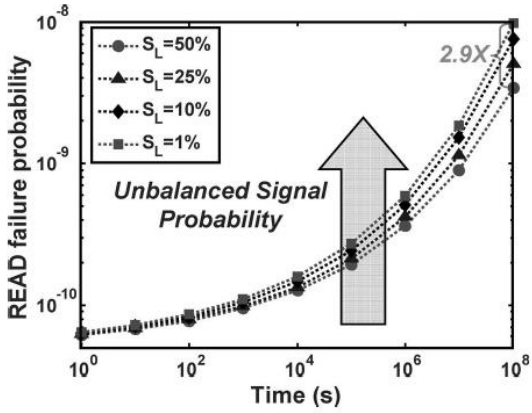


Fig.5. Read failure Probability under different signal probability [2].

P_{RF} increases when signal probability values are unbalanced.

Write ability of SRAM cell improves under NBTI degradation which means that it becomes easier to write the data to the SRAM cell. Write margin will decrease with time and around 88% reduction in probability of write failure is reported in [2] considering 3 years of stress time. PMOS transistor of the node storing a logic '1' undergoes NBTI degradation and this weakens the pull up thereby making the process of writing '0' to that node easier. Write margin reduction with time is an indicator for the improved write ability of 6T SRAM cell. Leakage of the SRAM cell affected by NBTI reduces because sub threshold leakage current depends exponentially on v_{th} as

$$I_{sub} \propto e^{(vgs-vth)/mVT}$$

Due to NBTI v_{th} increases and so threshold leakage current will also reduce. Yield of the SRAM array also gets affected under NBTI degradation. Yield relates to the number of chips that operates properly even after temporal degradation of NBTI [2]. Results of the yield measurement published in [2, 21] suggests that memory yield decreases under NBTI and shows dependence on the signal probability values. Balancing the signal probability can lead to the improvement in the memory yield.

VI. Strategies for Mitigating NBTI Degradation Effects in SRAM

In the earlier section, discussions were made on the NBTI induced performance degradation in 6T SRAM cell. Parameter which gets severely affected due to NBTI degradation includes RSNM, read failure probability and yield. Various design strategies have been proposed by researchers to reduce the effect of NBTI degradation on the performance of SRAM. This section deals with all such strategies that can be employed to combat against NBTI degradation in SRAM. These strategies can be categorized as follows:-

1. Controlling wordline voltage and duration [22]
2. Data flipping approach [19]
3. Optimal sizing of transistors [12,27,29]
4. Reliability monitor and body bias approach [33]
5. Supply voltage reduction [20,25]
6. Recovery boosting technique [24]

1. Controlling wordline voltage and duration:

Results published in [22] shows that both wordline voltage and duration are effective ways to mitigate NBTI effects in SRAM. NBTI induced degradation can be monitored by using reliability sensors and then the wordline pulse width can be adjusted to prevent data flipping by reading the data and then quickly disabling the wordlines. Wordline voltage modulation is also an effective way to mitigate NBTI degradation by increasing the time to flip the data or even eliminating the data flipping by mitigating the disturbance. Multiple SRAM cells should be included in the sensing block for better tracking the variations [22].

2. Data Flipping Approach:

A novel approach for recovering the SNM of SRAM cell has been proposed in [19]. Proposed approach implements data flipping of the cell periodically to balance the degradation of two PMOS devices. Flipping the cell contents after every 10^5 seconds can be performed either through software or hardware [19]. S/W approach flips the data periodically after every 10^5 seconds and during reading the data bits are inverted and are written back to the memory locations. This approach may not work for large cache size like for L3 cache which are few MBs in size. Hardware approach of data flipping involves some additional hardware and the data is flipped locally using inverters and is written back through multiplexers [19]. Read and write mechanism are required to be modified either using hardware approach or software approach so as to mitigate the effect of NBTI degradation in SRAM using bit flipping approach. The recovery in noise margin degradation caused due to NBTI can be up to 30% using bit flipping approach. Cell flipping approach tries to reduce the effect of NBTI degradation by balancing the signal probabilities at both sides of the cell [20]. This scheme is also not perfect because even with the balancing of signal probabilities RSNM can degrade by more than 10% [2, 20]. Fig.6 shows the reported degradation in SNM with signal probability and it clearly supports the fact that even balancing of the signal probabilities alone is not sufficient to combat against NBTI degradation in SRAM.

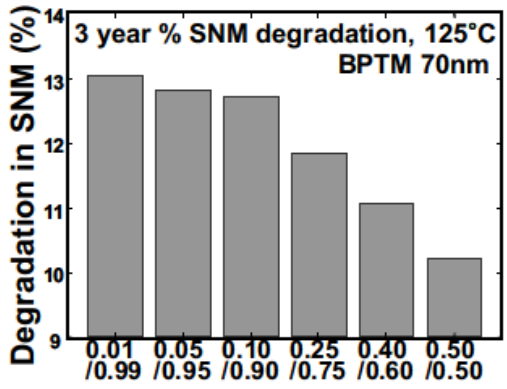


Fig.6. Effect of Signal Probability at MP2 and MP1 on SNM degradation in SRAM [2, 20].

3. Optimal Sizing of Transistors:

Sufficient margins in size can be provided when designing PMOS transistor, keeping NBTI degradation into consideration. Upsizing of PMOS transistor is an effective way to counter NBTI degradation but upsizing of PMOS will lead to additional area overhead. Upsizing the PMOS transistor in SRAM creates difficulty in device matching and also reduces noise margin [33]. Upsizing of PMOS transistor to combat NBTI degradation is an important issue and special algorithms like Genetic algorithm (GA) [27] and Lagrange Relaxation (LR) algorithm [12, 29] have proved to be extremely useful to correctly size the PMOS transistor without causing much performance degradation of the digital circuits. LR algorithm used in [12, 29] has been tested successfully on several ISCAS benchmark circuits and GA has been used to optimize the performance of domino logic circuits in [27]. These soft computing algorithms can be used in SRAM with well defined constraints in terms of noise margins to optimally size the PMOS transistor keeping NBTI degradation into account.

4. Reliability Monitor & Body Bias Approach

On chip reliability sensors can be employed to estimate the amount of degradation that is caused by NBTI in PMOS. Authors in [20, 33] suggest that ring oscillator can be used to predict the amount of NBTI induced degradation and then appropriate body bias can be applied to counter the degradation. PMOS gate voltage is made more negative during stress and so only positive forward bias is applied to mitigate this change [33]. The magnitude of the applied forward bias depends on the NBTI stress amount. If ring oscillator is used to determine the extent of NBTI degradation then phase comparator is used to compare the frequency of the undegraded ring oscillator and degraded ring oscillator. Fig.7 shows the design of a reliability sensor made using

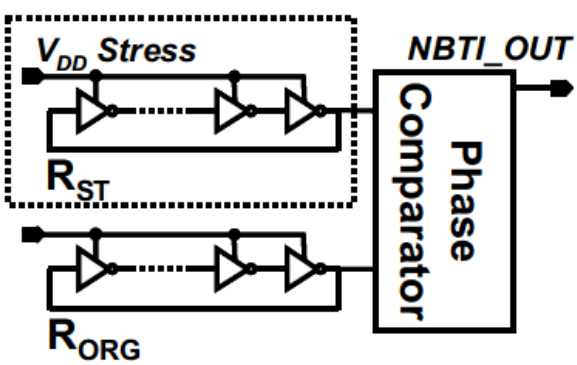


Fig.7. Reliability Sensor using Ring Oscillator [20].

ring oscillator and phase comparator. The corrective body bias will depend on the output signal of the phase comparator. Phase Locked Loop (PLL) can also act as a good reliability sensor.

5. Supply Voltage Reduction:

Supply voltage reduction in standby mode will lead to decrease in the value of oxide electric field (Eox) which reduces the effect of NBTI. This strategy of v_{dd} reduction can be easily implemented in existing memory design without much additional overhead [20]. Voltage reduction in standby mode is also utilized for leakage reduction in SRAM design. Degradation in terms of SNM is not much when v_{dd} reduction is done in standby mode. Experimental results published in [25] shows that under lower v_{dd}, transistors and circuit performance become more sensitive to stress induced v_{th} shift and even a small degradation in v_{th} can result in larger timing degradation.

6. Recovery Boosting Technique:

A novel approach for recovery boosting is proposed in [24] in which slight modification in SRAM cell design is made to ensure that both PMOS transistors in the SRAM cell can be put into the recovery mode. Modified SRAM cell design for recovery boosting is shown in Fig.8

Both PMOS devices in SRAM are put to recovery mode by raising the ground potential to vdd by making CR signal '0' and both BL and BLB lines are precharged to vdd. Recovery boosting technique is applied to issue queue and simulation results show that up to 56% improvement in SNM can be achieved for the issue queue without compromising much on other performance parameters.

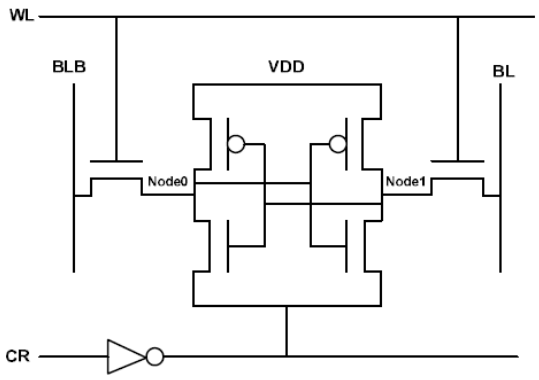


Fig.8. Recovery Boosting Technique [24].

VII. Conclusions

This paper reviews NBTI ageing degradation and its mechanism based on RD framework. Different models proposed in the literature to predict v_{th} degradation due to NBTI have been investigated in detail. Different assumptions and highlighting points for predicting v_{th} shift that is caused due to NBTI have been explored. Review suggests that it is important to consider the effect of bulk interface traps and role of nitrogen and boron at interface so as to accurately predict the v_{th} shift caused due to NBTI. Effect of NBTI on the performance of 6T SRAM cell has been investigated and literature suggests that RSNM and v_{min} degrades severely due to NBTI. Strategies for mitigating the NBTI degradation effects from SRAM have also been discussed. Deploying NBTI monitors to estimate the amount of NBTI degradation can be very useful and according to the o/p of NBTI monitor corrective measures can be taken to protect the failure of VLSI chip. Existing design techniques that are used to combat against NBTI degradation in SRAM perform well but still there is a scope of improvement in terms of improving the SRAM cell performance metrics like SNM & Read failure probability under NBTI degradation. Design Techniques utilized to reduce the vulnerability of SRAM to NBTI must be efficient in terms of area, power and other performance parameters with minimal modification in the SRAM cell design.

References

[1] M.A. Alam, S. Mahapatra, "A Comprehensive Model of PMOS NBTI degradation", Elsevier, Microelectronics Reliability, vol.45, pp.71-81, 2005.

[2] Kunhyuk Kang, Haldun Kufluoglu, Kaushik Roy, Muhammad Ashraful Alam, "Impact of Negative-Bias Temperature Instability in Nanoscale SRAM Array:Modeling and Analysis", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, vol.26, no.10, pp.1770-1780, Oct. 2007.

[3] Deal BE, Sklar M, Grove AS, Snow EH, "Characteristics of the surface-state charge(Qss) of thermally oxidized silicon", JElectrochem Soc, 1967;114:266.

[4] Jeppson KO, Svensson CM, "Negative bias stress of MOS devices at high electric fields and degradation of MOS devices", J Appl Phys 1977;48:2004-14.

[5] Kimizuka N, Yamamoto T, Mogami T, Yamaguchi K, Imai K, Horiuchi T, " The impact of bias temperature instability for direct tunneling ultra-thin gate oxide on MOSFET scaling", In: Proc VLSI Tech Symp, 1999.pp.73-4.

[6] Schroder DK, Babcock JA, " Negative bias temperature instability:road to cross in deep submicron semiconductor manufacturing", Appl Phys Lett 2003;94:1-18.

[7] Sarvesh Bhardwaj, Wenping Wang, Rakesh Vattikonda, Yu Cao, Sarma Vrudhula, " Predictive Modeling of the NBTI Effect for Reliable Design", IEEE 2006 Custom Integrated Circuits Conference, pp. 189-192, 2006.

[8] Haldun Kufluoglu, Muhammad Ashraful Alam, "A Generalised Reaction- Diffusion Model With Explicit H-H_2 Dynamics for Negative- Bias Temperature-Instability (NBTI) Degradation", IEEE Transactions on Electron Devices, vol.54, no. 5, pp.1101-1107, May 2007.

[9] Wenping Wang, Vijay Reddy, Anand T. Krishnan, Rakesh Vattikonda. Srikanth Krishnan, Yu Cao, " Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology", IEEE Transactions on Device and Materials Reliability, vol.7, no.4, pp.509-517, Dec. 2007.

[10] Rakesh Vattikonda, Wenping Wang, Yu Cao, "Modeling and Minimization of PMOS NBTI Effect for Robust Nanometer Design", in Proc.Des.Autom. Conf.,2006, pp.1047-1052.

[11] A.T.Krishnan, V.Reddy, S.Chakravarthi, J.Rodriguez, S.John, S.Krishnan, "NBTI impact on transistor and circuit:Models, mechanisms and scaling effects", in proc.iedm,2003,pp.14.5.1-14.5.4

[12] Bipul C.Paul, Kunhyuk Kang, Haldun Kufluoglu, Muhammad A. Alam, Kaushik Roy, "Negative Bias Temperature Instability:Estimation and Design for Improved Reliability of Nanoscale Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol.26,no.4,pp.743-751, April 2007.

[13] J.H. Stathis, S.Zafar, "The negative bias temperature instability in MOS devices: A review", Microelectronics Reliability 46 (2006) 270-286.

[14] H.Hussin, N.Soin, N.M.Karim, S.F. Wan Muhamad Hatta, "On the effects of NBTI degradation in p-MOSFET devices", Physica B 407 (2012) 3031-3033.

[15] R.Wittman, H.Puchner, L.Hinh, H.Ceric, A.Gehring, S.Selberherr, "Simulation of Dynamic NBTI Degradation for a 90nm CMOS Technology", NSTI-NanoTech 2005 vol.3, pp.29-32, 2005.

[16] Luo Yong, Huang Daming, Liu Wenjun, Li Mingfu, "Boundary condition and initial value effects in the reaction-diffusion model of interface trap generation/recovery", Journal of Semiconductors, vol.30, no.7,074008-1 -074008-6, July 2009.

[17] G.Chen, M.F.Li, C.H. Ang, J.Z. Zheng, D.L. Kwong, "Dynamic NBTI of p-MOS Transistors and Its Impact on MOSFET Scaling", IEEE Electron Device Letters, pp.1-3, 2002.

[18] 2Dieter K. Schroder, "Negative bias temperature instability:What do we understand?", Microelectronics Reliability 47 (2007) 841-852.

[19] Sanjay V.Kumar, Chris H.Kim, and Sachin S. Sapatnekar, "Impact of NBTI on SRAM Read Stability and Design for Reliability",Proc. Int. Symp. Quality Electon.Des, 2006.

[20] Kunhyuk Kang, Sakshi Gangwal, Sang Phill Park and Kaushik Roy, "NBTI Induced Performance Degradation in Logic and Memory Circuits:How Effectively Can We Approach a Reliability Solution?", ASP-DAC '08 Proceedings of the 2008 Asia and South Pacific Design Automation Conference, pp.726-731.

[21] S.Drapatz, G.Georgakos, D.Schmitt, "Impact of negative and positive bias temperature stress on 6T–SRAM cells", Advances in Radio Science, 7, pp.191-196, 2009.

[22] Tony Tae-Hyoung Kim, Zhi Hui Kong, "Impact Analysis of NBTI/PBTI on SRAM V_{MIN} and Design Techniques for Improved SRAM $V_{MIN.}$", Journal of Semiconductor Technology and Science, vol.13,no.2,pp.87-97, April 2013.

[23] N.Goel, P.Dubey,J.Kawa, S.Mahapatra, "Impact of Time-Zero and NBTI Variabaility on Sub-20nm FinFET based SRAM at Low Voltages", IRPS 2015, IEEE,pp. CA.5.1-CA.5.7.

[24] Taniya Siddiqua and Sudhanva Gurumurthi, "Recovery Boosting: A Technique to enhance NBTI recovery in SRAM Arrays", ISVLSI, 2010 IEEE Computer Society Annual Symposium pp.393-398.

[25] Wenping Wang, Shengqi Yang, Sarvesh Bharadwaj, Rakesh Vattikonda, Sarma Vrudhula, Frank Liu, Yu Cao, "The Impact of NBTI on the Performance of Combinational and Sequential Circuits", DAC 2007, Proceedings of the 44th annual design automation conference, pp.364-369.

[26] Masaoud Houshmand Kaffashian, Reza Lotfi, Khalil Mafineezhadand, Hamid Mahmoodi, " An optimization method for NBTI-aware design of domino logic circuits in nano-scale CMOS", IEICE Electronics Express, vol.8, no.17, pp.1406-1411.

[27] Yao Wang, Sorin Cotofana, Liang Fang, " A Unified Aging Model of NBTI and HCL Degradation towards Lifetime Reliability Management for Nanoscale MOSFET Circuits", Nanoscale Architectures (NANOARCH), 2011 IEEE/ACM International Symposium, pp. 175 – 180.

[28] Bipul C Paul, Kunhyuk Kang, Haldun Kufluoglu, Muhammad Ashraful Alam and Kaushik Roy, " Temporal Performance Degradation under NBTI: Estimation and Design for Improved Reliability of Nanoscale Circuits", EDAA 2006.

[29] Benton H. Calhoun, Anantha Chandrakasan, " Analyzing Static Noise Margin for Sub-threshold SRAM in 65nm CMOS", ESSCIRC, Grenoble, France, 2005.

[30] Evert Seevinck, Frans J. List, Jan Lohstroh, " Static – Noise Margin Analysis of MOS SRAM Cells", IEEE Journal of Solid –State Circuits, vol.sc-22, no.5, pp.748-754, Oct. 1987.

[31] Saibal Mukhopadhyay, Hamid Mahmoodi, Kaushik Roy, " Reduction of Parametric Failures in Sub-100-nm SRAM Array Using Body Bias", IEEE Transcations on Computer –Aided Design of Integrated Circuits and Systems, vol.27, no.1, pp.174-183, Jan.2008.

[32] Zhenyu (Jerry) Q, Mircea R. Stan, " NBTI Resilient Circuits Using Adaptive Body Biasing", GLSVLSI'08, ACM 978-1-59593-999-9/08/05, pp.285-290.

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