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## Design of Adder Using Quantum Cellular Automata

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### Abstract

QCA is the trending technologies for designing less hardware and low power consumed circuits measured in Nano-scale. These QCA cells are accustomed to construct combinational and sequential circuits. In this paper we presented a design for developing a basic arithmetic unit called full adder using Quantum cellular automata. The new submitted FA consists fewer amounts of quantum cells and delay also minimizes, when compared with the existing architecture.

**Index Terms:** Full adder (FA), Majority Gate (MG). QCA cell.

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### 1. Introduction

QCA were introduced by Lent C.S. and Tougaw. P.D [1]. This technology consumes very less area, low power dissipation, less leakage current. This technology made of six come up technologies regarding future computers. In [3], it explains logical expressions implemented by utilizing majority gates (MG) and inverters. In [2], it explains how to implement QCA circuits using majority gate and inverter gate. With these we can implement basic circuits, adders [4], mux [6,7], flip-flops [5], etc...

Adders are the fundamental element in the ALU's and Multiplications Units. The adder block is implemented by XOR, AND logic gates which performs binary arithmetic operations. Conceiving a latest adder design utilizing QCA technology do a leading part in majority of the integrated circuit design. QCA consists of quantized cells, composed of 4 quantum dots located at the edges of the basic quantum cell shown in fig1. The electronic charge is confined in the polarized dots. The polarized electrons can tunnel in to the dots which are diagonal placed because of columbic repulsion. But they cannot tunnel in to the adjacent cells because of

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potential barrier exists in the middle of the adjacent dots.

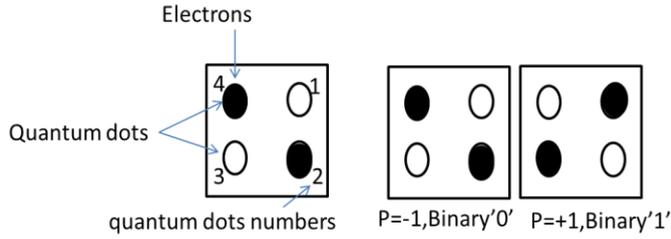


Fig.1. Basic Quantum Cellular Automata Structure

The 2 quantum dots and 2 electrons arrangement of a basic QCA structure is represented in the fig1. The expression of the polarization(P) of the quantum cell is shown in eq.1 [8]. P=-1 is represented as binary logical value '0' and P=+1 is represented as binary logical value '1' [16, 17], as shown in the fig.1.

$$P = \frac{(P1 + P3) - (P2 + P4)}{P1 + P2 + P3 + P4} \tag{1}$$

Here p1, p2, p3, p4 designates the electrons that are located in the QCA basic structure. All the digital circuit designs are formulated utilizing QCA

QCA circuits are formulated utilizing majority gate which comprise of 5 QCA cells, out of which 3 are inputs, 1 output and 1 processing cell shown in the fig.2.

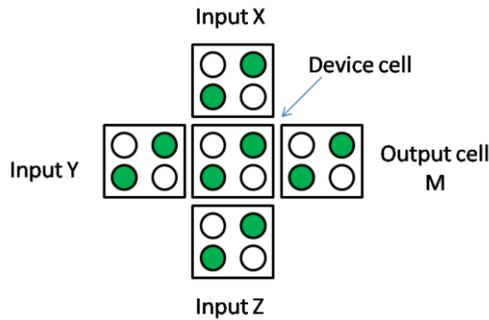


Fig.2. Majority Gate of 5 cells QCA

The logical expression of an MG is given in the eq.2.

$$f(a,b,c) = a.b + b.c + c.a \tag{2}$$

Designing digital circuits can be done by utilizing majority gates. From eq.2 one of the input is zero i.e assume c='0', then the majority gate works as a logical AND gate shown in fig.3.

$$f(a,b,0) = a.b \tag{3}$$

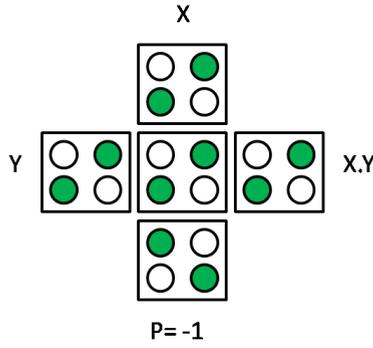


Fig.3 QCA design for an AND Gate

From eq.2 if  $c=1$ , then the MG works as a logical OR gate shown in fig.4

$$f(a,b,1) = a + b \tag{4}$$

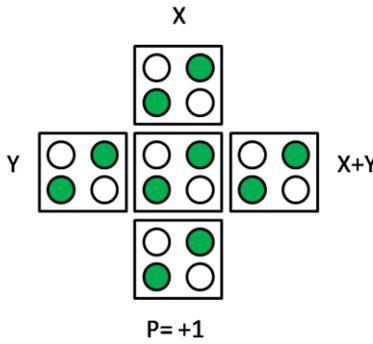


Fig.4 QCA design for an OR Gate

The QCA design for an inverter which is shown in fig.5

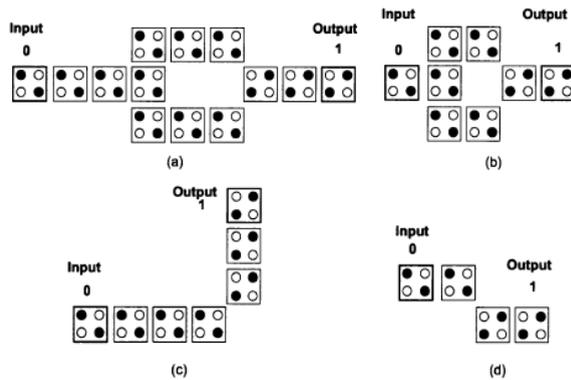


Fig.5 QCA design for an inverter

**2. Literature Survey for the adder Design using QCA**

A full adder is a design which adds 3 binary inputs and obtain 2 outputs Sum and Carry. The formulae for sum and carry using majority gates is given in eq.5 and eq.6. Finally, full adder structure requires five majority gates and three basic inverters [9] which is shown in fig.6.

$$Carry = f(a, b, c) \tag{5}$$

$$Sum = f(f(a', b, c), f(a, b', c), f(a, b, c')) \tag{6}$$

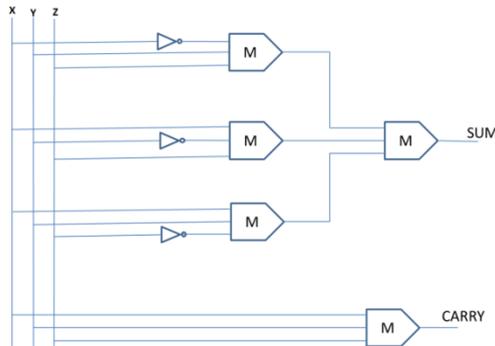


Fig.6 Basic Full adder using Majority gates

K. Navi [10] has proposed different logical expression which is given in the eq.7 ,eq.8 and its logical diagram is shown in fig.7.

$$Carry = f(a, b, c) \tag{7}$$

$$Sum = f(carry', carry', a, b, c) \tag{8}$$

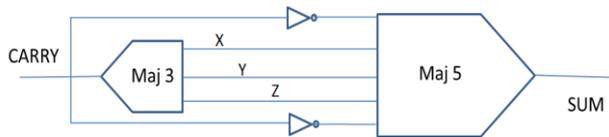


Fig.7. [10] Full adder QCA design

From [10] adders is developed by utilizing 3 input XOR gate [18] and five input majority gate. The 3 input XOR based on QCA is shown in fig.8 comprising 14 cells and assign one of the input is zero which behaves as an XOR gate.

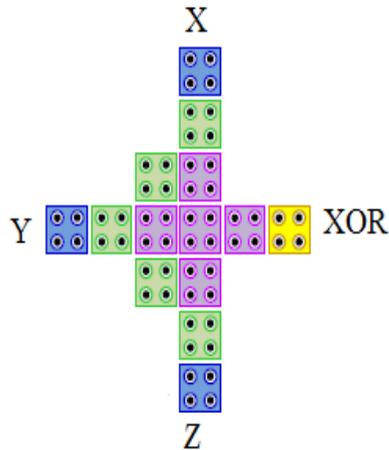


Fig.8. [18] 3-input XOR gate QCA design

### 3. Proposed design for Full adder using QCA

The structural design of the proposed design which comprising of 3 input majority gate and an XOR gate is shown in fig.9. The proposed design has 23 standard cell structure by using 2 clocks is shown in fig.10. Blue color represents full adder inputs, yellow color designated outputs and the remaining colors related to setup, hold, relax and release phases

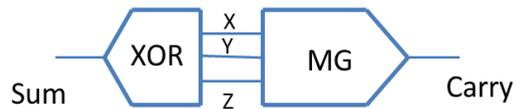


Fig.9 Proposed Full adder using 3 input XOR gate and majority gate



Fig.10. Proposed Full adder design using QCA

#### 4. Simulated Results for the proposed adder

The possible output and input combinations are shown in fig.11.

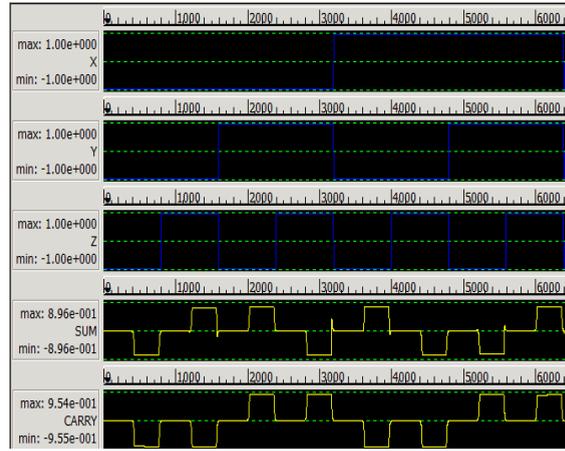


Fig.11. Simulated results of the waveform of proposed FA.

Table I shows the comparative analysis of full adder design using QCA. From Ref [8] the full adder has been constructed using 38 standard cell structure in which delay is more [11]. The proposed design requires the 23 standard QCA cell structure has better performance in terms of area and delay.

Table1. Comparative Analysis of QCA based Full adder design

Circuit	No.of QCA cells	Area in Nano square meters	No.of Clock Phases
In Ref. [9]	192	190244	4
In Ref. [12]	145	179901	4
In Ref. [13]	107	115781	4
In Ref. [14]	61	40512	3
In Ref. [15]	51	37054	3
In Ref. [8]	38	30568	3
In Ref. [11]	31	23598	2
New Structure	23	16284	2

#### 5. Conclusions

The new structure for QCA based full adder which occupies less area in terms of QCA cell structures, number of clock phases, Area in Nano square meters compared to the other full adder architectures mentioned in the literature. The limitation for the proposed design is unable to reduce the number of clock because data transfer will not takes place.

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